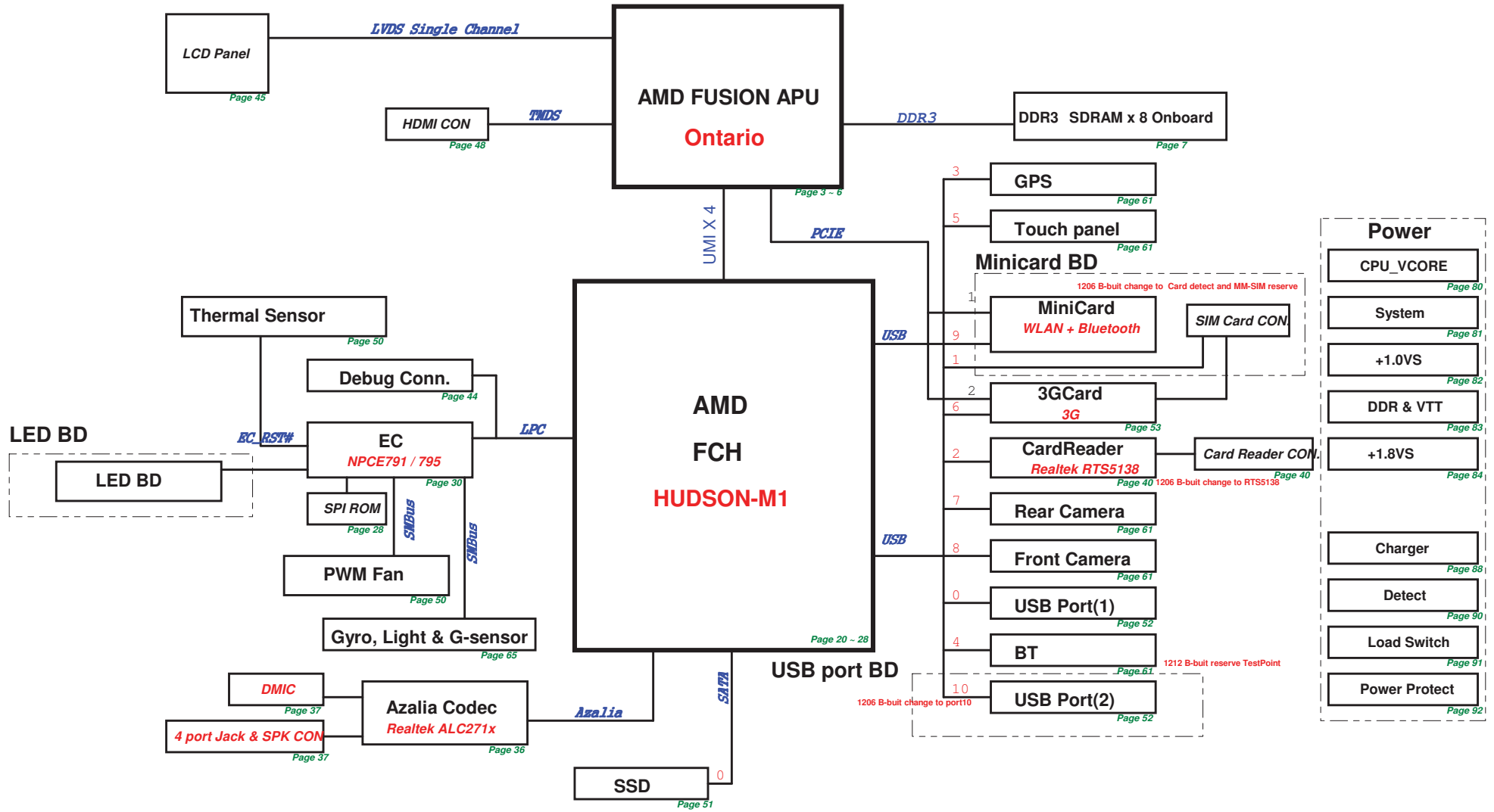


Armani EAB00 AMD Brazos Platform Rev. 2.0

BLOCK DIAGRAM



FCH Hudson M1	Use As	Signal Name	INT/EXT Pull-up/down	Power
General Events				
GA20IN/GEVENT0#	GPI	A20GATE	INT PU 8.2K	+3VS
KBRST#/GEVENT1#	GPI	EC_KB_RST#	INT PU 8.2K	+3VS
THRMTTRIP#/GEVENT2#	GPI	CPU_THERMTTRIP#	INT PU 10K	+3VSUS
LPC_PME#/GEVENT3#	GPI	EXT_SCI# @		+3VSUS
PCI_PME#/GEVENT4#	GPI	EXT_SMI# @		+3VSUS
SPI_CS3#/GBE_STAT1/GEVENT21#	GPI	EXT_SCI#	INT PU 10K	+3VSUS
RI#/GEVENT22#	GPI	EXT_SMI#	INT PU 10K	+3VSUS
GEVENT5#	GPI	USB30_EXT_SMI#	INT PU 10K	+3VSUS
WAKE#/GEVENT8#	GPI	PCIE_WAKE#	INT PU 10K	+3VSUS
USB_OC3#/AC_PRES/TDO/GEVENT15#		SATA_ODD_PRSNT#	INT PU 10K	+3VSUS
USB_OC4#/IR_RX0/GEVENT16#		SATA_ODD_DA#	INT PU 10K	+3VSUS
SLP_S3#	GPO	PM_SUSB#	EXT PD 100K	+3VSUS
SLP_S5#	GPO	PM_SUSC#	EXT PD 100K	+3VSUS
PWR_BTN#	GPI	PM_PWRBTN#		+3VSUS
PWR_GOOD	GPI	PM_PWROK		+3VSUS
RSMRST#	GPI	PM_RSMRST#	EXT PD 10K	+3VSUS
NB_PWRGD		NB_PWRGD	EXT PU 4.7K	+3VSUS
GPIO				
INTH#/GPIO35		VGA_PWRON	EXT PU 8.2K	+3VS
SCLO/GPIO43		SMB_CLK_S	EXT PU 2.2K	+3VS
SDA0/GPIO47		SMB_DAT_S	EXT PU 2.2K	+3VS
SERIRQ/GPIO48		INT_SERIRQ	INT PU 8.2K	+3VS
FANOUT0/GPIO53	GPO	WLAN_ON	INT PU 8.2K	+3VS
SATA_IS4#/FANOUT3/GPIO55	Native	SATA_ODD_PWRGT	INT PU 8.2K	+3VS
CLK_REQ1#/FANOUT4/GPIO61	Native	CLKREQ_MINICARD_WLAN#	EXT PD 10K @	+3VS
CLK_REQ2#/FANIN4/GPIO62	Native	CLKREQ2_LAN#	EXT PD 10K @	+3VS
CLKREQ3#/SATA_IS1#/GPIO63	Native	CLKREQ_PCIE_USB30#	EXT PD 10K @	+3VS
CLK_REQ4#/SATA_ISO#/GPIO64	Native	CLK_REQ4#_DP	EXT PD 10K	+3VS
CLK_REQG#/GPIO65/OSCIN/IDLEEXT#	Native	ATI_CLKREQ#	INT PU 8.2K	+3VS
SPKR/GPIO66		SB_SPKR	-	+3VS
SATA_ACT#/GPIO67		SATA_LED#	EXT PU 10K	+3VS
SPI_CLK/GPIO162		SPI_CLK	INT PD 10K	+3VSUS
SPI_DO/GPIO163		SPI_DO	INT PD 10K	+3VSUS
SPI_DI/GPIO164		SPI_DI	INT PD 10K	+3VSUS
SPI_CS1#/GPIO165		SPI_CS1#	INT PD 10K	+3VSUS
AZ_SDIN0/GPIO167		ACZ_SDIN0	EXT PD 10K @	+3VSUS
AZ_SDIN0/GPIO168		ACZ_SDIN1	EXT PD 10K @	+3VSUS
AZ_SDIN0/GPIO169		ACZ_SDIN2	EXT PD 10K @	+3VSUS
TEMPIN0/GPIO171			EXT PD 10K	+3VSUS
TEMPIN1/GPIO172			EXT PD 10K	+3VSUS
TEMPIN2/GPIO173			EXT PD 10K	+3VSUS
TEMPIN3/TELETRIP#/GPIO174		APU_ALERT#		+3VSUS
VIN0/GPIO175			EXT PD 10K	+3VSUS
VIN1/GPIO176			EXT PD 10K	+3VSUS
VIN2/GPIO177			EXT PD 10K	+3VSUS
VIN3/GPIO178			EXT PD 10K	+3VSUS
VIN4/GPIO179			EXT PD 10K	+3VSUS
VIN5/GPIO180			EXT PD 10K	+3VSUS
VIN6/GBE_STAT3/GPIO181			EXT PD 10K	+3VSUS
VIN7/GBE_LED3/GPIO182			EXT PD 10K	+3VSUS
USB_FSD0P/GPIO185		USB_CB0	INT PD 15K	+3VSUS
USB_FSD0P/GPIO186		USB_CB1	INT PD 15K	+3VSUS
PS2_DAT/SDA4/GPIO187		WLAN_LED	INT PU 10K	+3VSUS
SCL2/GPIO193			EXT PD 10K	+3VSUS
SDA2/GPIO194			EXT PD 10K	+3VSUS
SCL3_LV/GPIO195			EXT PD 10K	+3VSUS
SDA3_LV/GPIO196			EXT PD 10K	+3VSUS
EC_PWM2/EC_TIMER2/GPIO199		EC_PWM2	EXT PU 10K	+3VSUS
EC_PWM3/EC_TIMER3/GPIO200		EC_PWM3	EXT PD 2.2K @	+3VSUS
KSI_0/GPIO209		USB_SEL (DOS:1/WIN:0)	INT PU 10K	+3VSUS
KSO_1/GPIO210		BT_ON	INT PU 10K	+3VSUS
SCL1/GPIO227			EXT PD 10K	+3VSUS
SDA1/GPIO228			EXT PD 10K	+3VSUS

EC GPIO	Use As	Signal Name
GPIO0		RTCCLK
GPIO1		FAN0_TACH
GPIO2		-
GPIO3		PWR_SW#
GPIO4		BAT1_IN_OC#
GPIO5		AC_IN_OC
GPIO6		DC_IN_LED#
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		SUSB_EC#
GPIO11		PM_CLKRUN#
GPIO12		-
GPIO13		PM_PWROK
GPIO14		USB_OC2#_EC
GPIO15		PWR_GREEN_LED#
GPIO16		-
GPIO17		SMB0_CLK
GPIO18		-
GPIO19		-
GPIO20		USB_OC1#_EC
GPIO21		PWR_AMBER_LED#
GPIO22		SMB0_DAT
GPIO23		PLT_ID0
GPIO24		-
GPIO25		-
GPIO26		TP_CLK
GPIO27		TP_DAT
GPIO28		-
GPIO29		-
GPIO30		VSUS_ON
GPIO31		EC_LPCRST_GATE
GPIO32		LCD_BL_PWM
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		NUM_LED#
GPIO37		-
GPIO38		-
GPIO39		-
GPIO40		BAT_WHITE_LED#
GPIO41		TP_ON_OFF#
GPIO42		PM_PWRBTN#
GPIO43		PM_RSMRST#
GPIO44		ALL_SYSTEM_PWRGD
GPIO45		BAT_ORG_LED#
GPIO46		-
GPIO47		PM_SUSC#
GPIO48		-
GPIO49		-
GPIO50		LCD_BACKOFF#
GPIO51		CAP_LED#
GPIO52		THRO_CPU
GPIO53		SUS_PWRGD
GPIO54		EXT_SCI#
GPIO55		-
GPIO56		PLT_ID1
GPIO57		KSO17
GPIO58		-
GPIO59		-
GPIO60		KSO16
GPIO61		KSO15
GPIO62		KSO14
GPIO63		KSO13
GPIO64		KSO12
GPIO65		EXT_SMI#
GPIO66		FAN_PWM

EC GPIO	Use As	Signal Name
GPIO67		SUSC_EC#
GPIO68		-
GPIO69		-
GPIO70		OP_SD#
GPIO71		PM_SUSB#
GPIO72		LID_SW#
GPIO73		SMB1_CLK
GPIO74		SMB1_DAT
GPIO75		-
GPIO76		SHBM
GPIO77		-
GPIO78		-
GPIO79		-
GPIO80		-
GPIO81		CPU_VRON
GPIO82		USBSLP_EN#
GPIO83		-
GPIO84		USBP01_EN#
GPIO85		A20GATE
GPIO86		RCIN#
GPIO87		-
GPIO88		-
GPIO89		-
GPIO90		AD_IINP
GPIO91		-
GPIO92		-
GPIO93		-
GPIO94		-
GPIO95		-
GPIO96		CTL_FAN
GPIO97		VRM_PWRGD

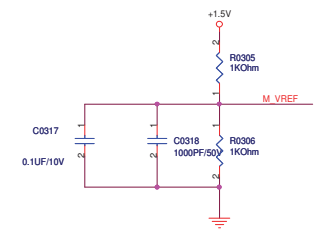
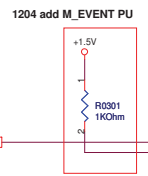
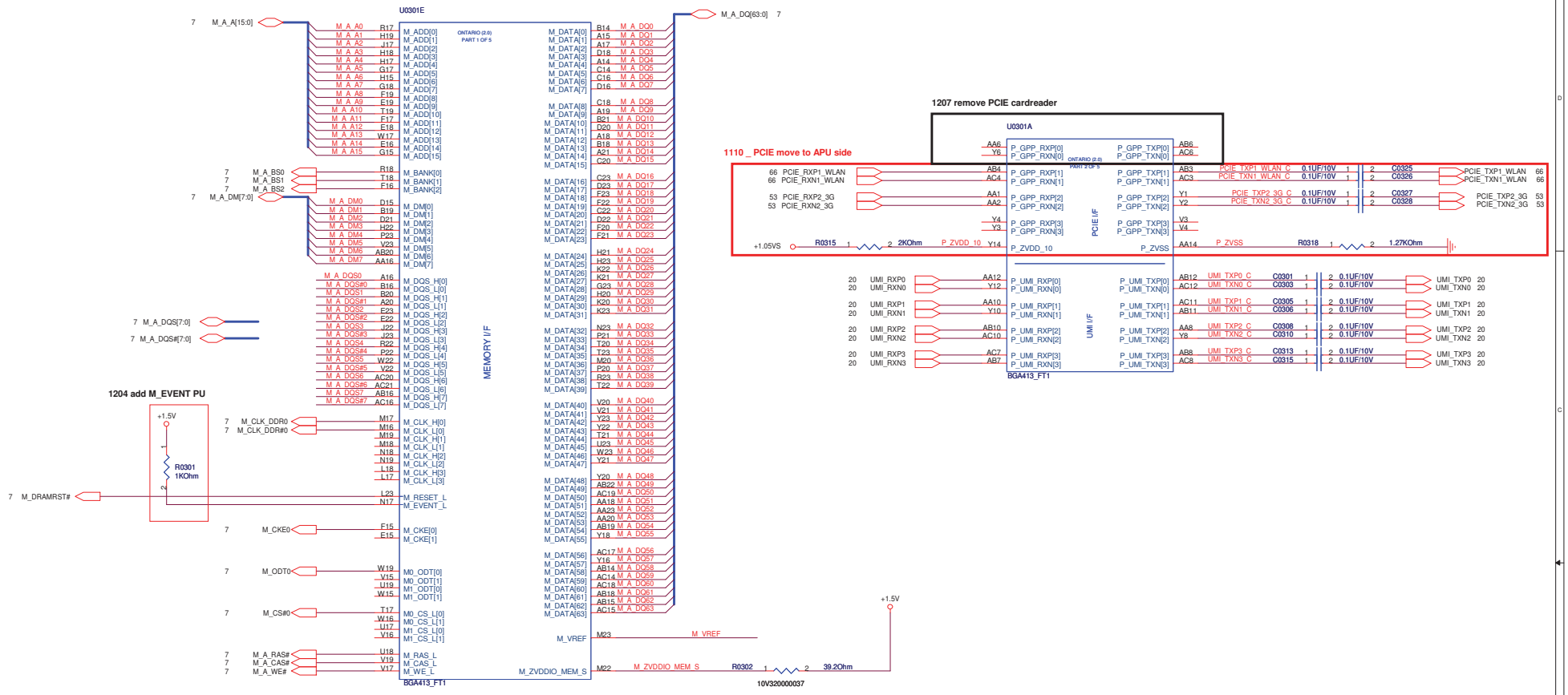
SM BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	101000x (A0h)
SO-DIMM 1	1010001x (A4h)
CPU Thermal IC(G780)	1001100x (98h)
VGA Thermal IC(G781-1)	1001100x (9Ah)

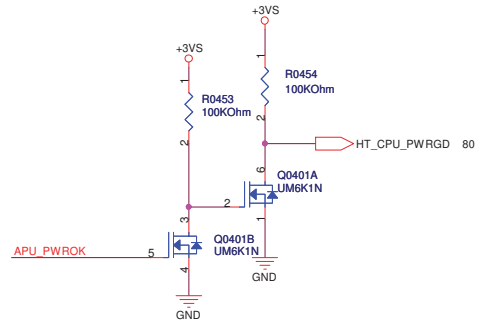
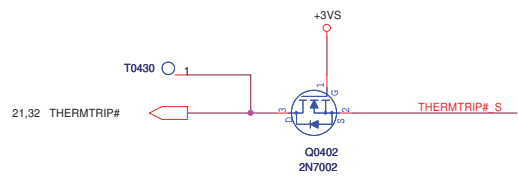
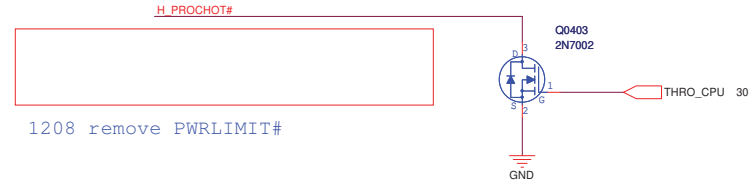
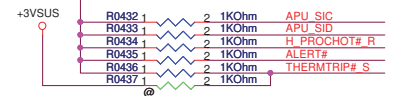
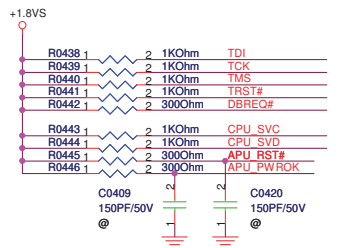
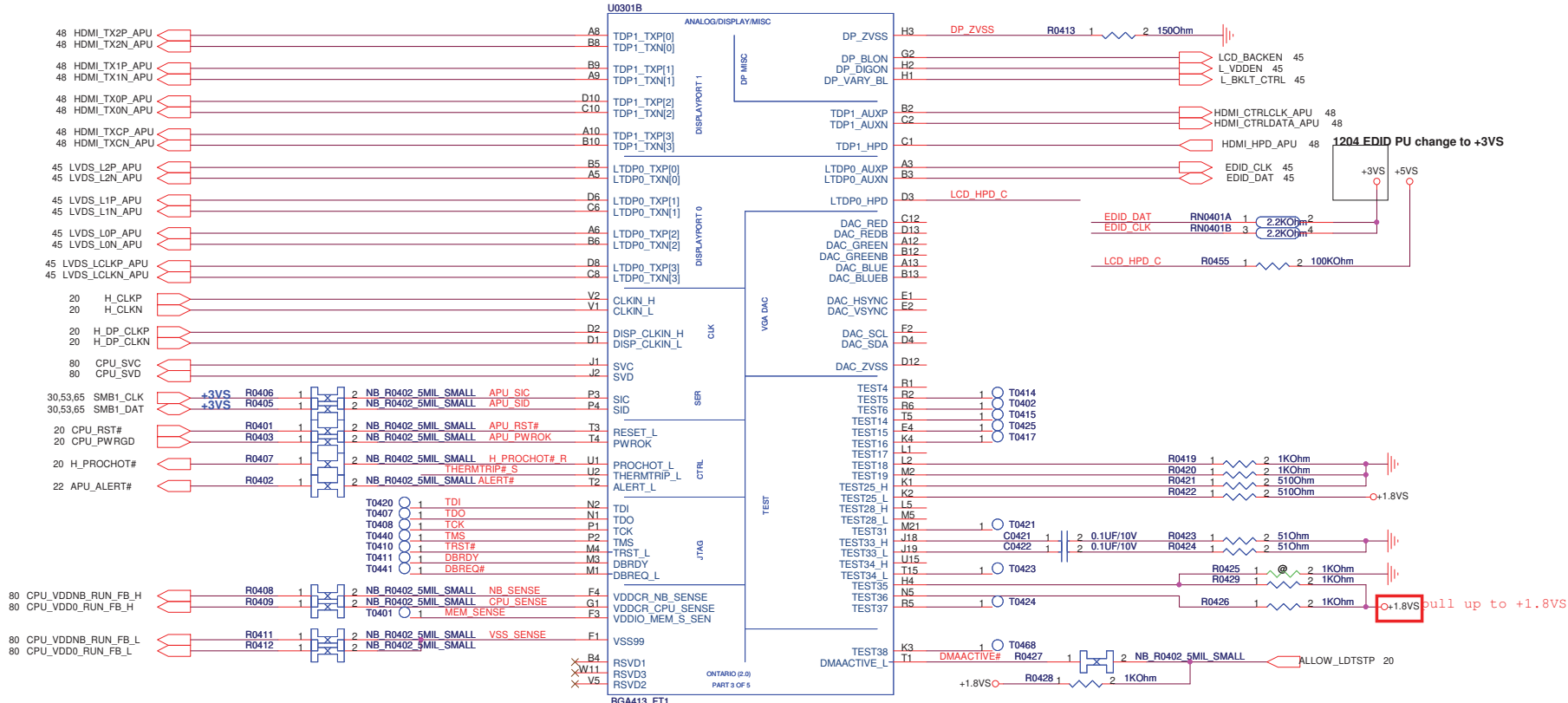
APU	DP0	LVDS	USB 0	USB Port (1)
				USB 1
			USB 2	USB Port (3)
			USB 3	USB Port (4)
			USB 4	N/A
			USB 5	N/A
			USB 6	N/A
			USB 7	Card Reader
			USB 8	CMOS Camera
			USB 9	Bluetooth
			USB 10	N/A
			USB 11	N/A
			USB 12	N/A
			USB 13	N/A

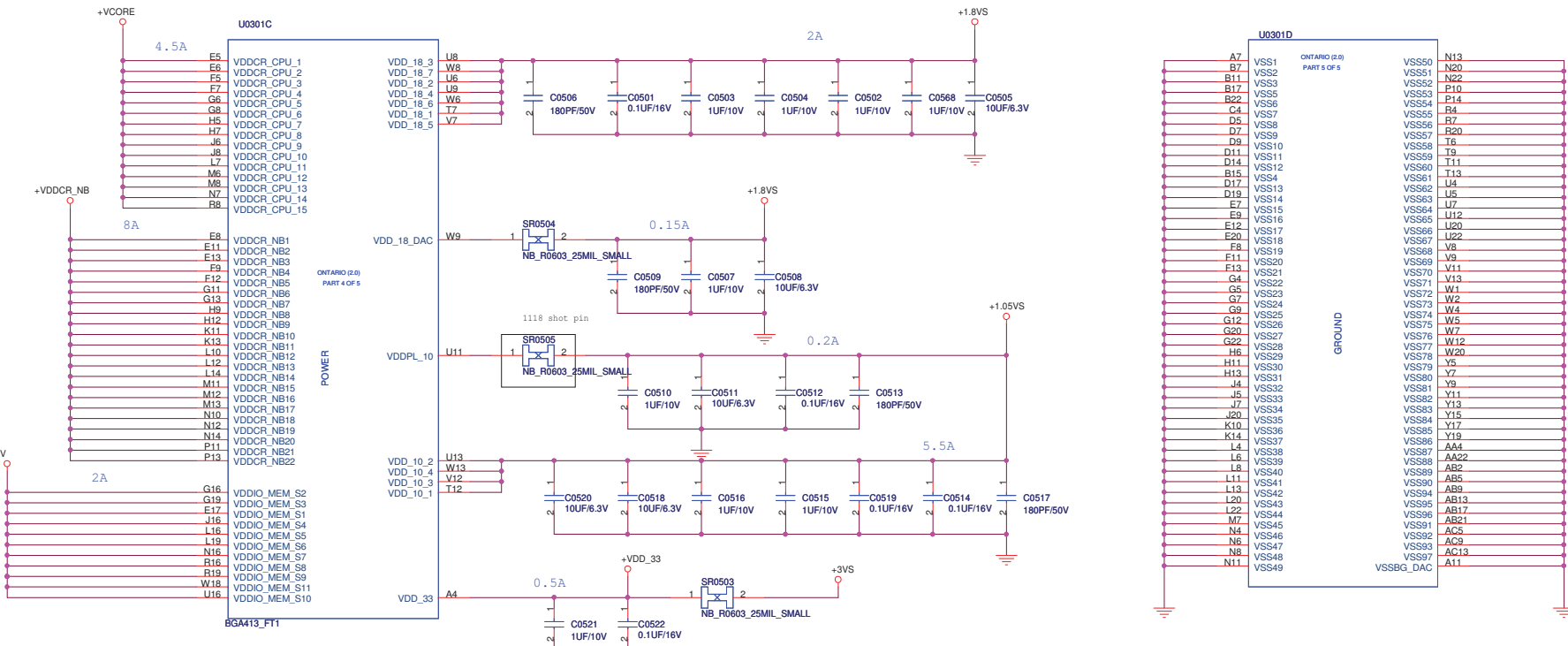
FCH	DP1	HDMI
GPP0	N/A	
GPP1	WLAN	
GPP2	LAN	
GPP3	USB3.0_NEC	
GPP4	N/A	
GPP5	N/A	

SATA0	SATA HDD
SATA1	N/A
SATA2	N/A
SATA3	N/A
SATA4	N/A
SATA5	N/A



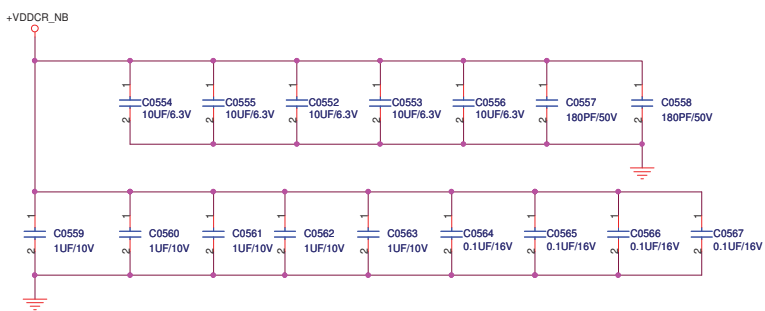
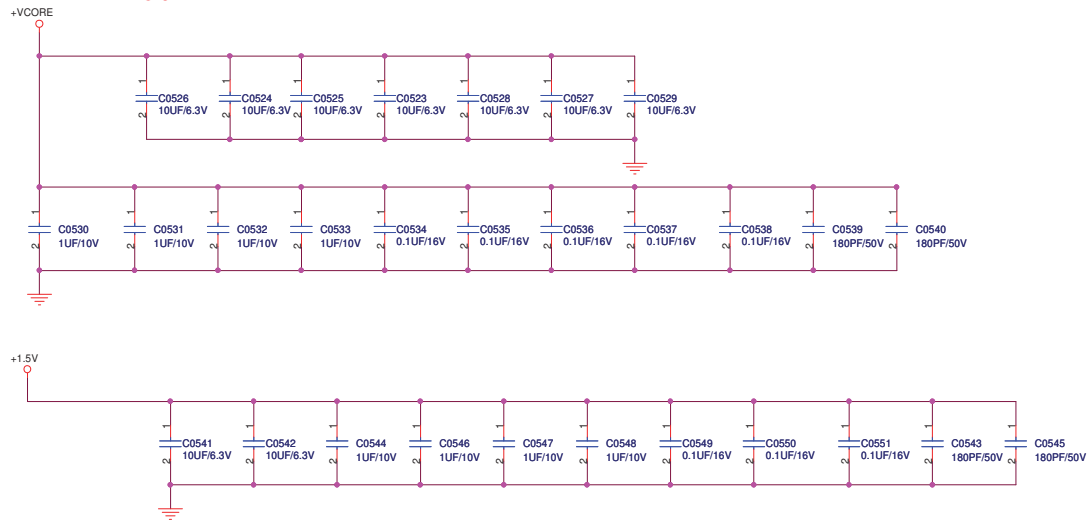
place within 1000mils with APU





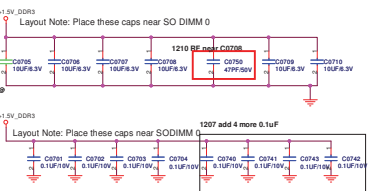
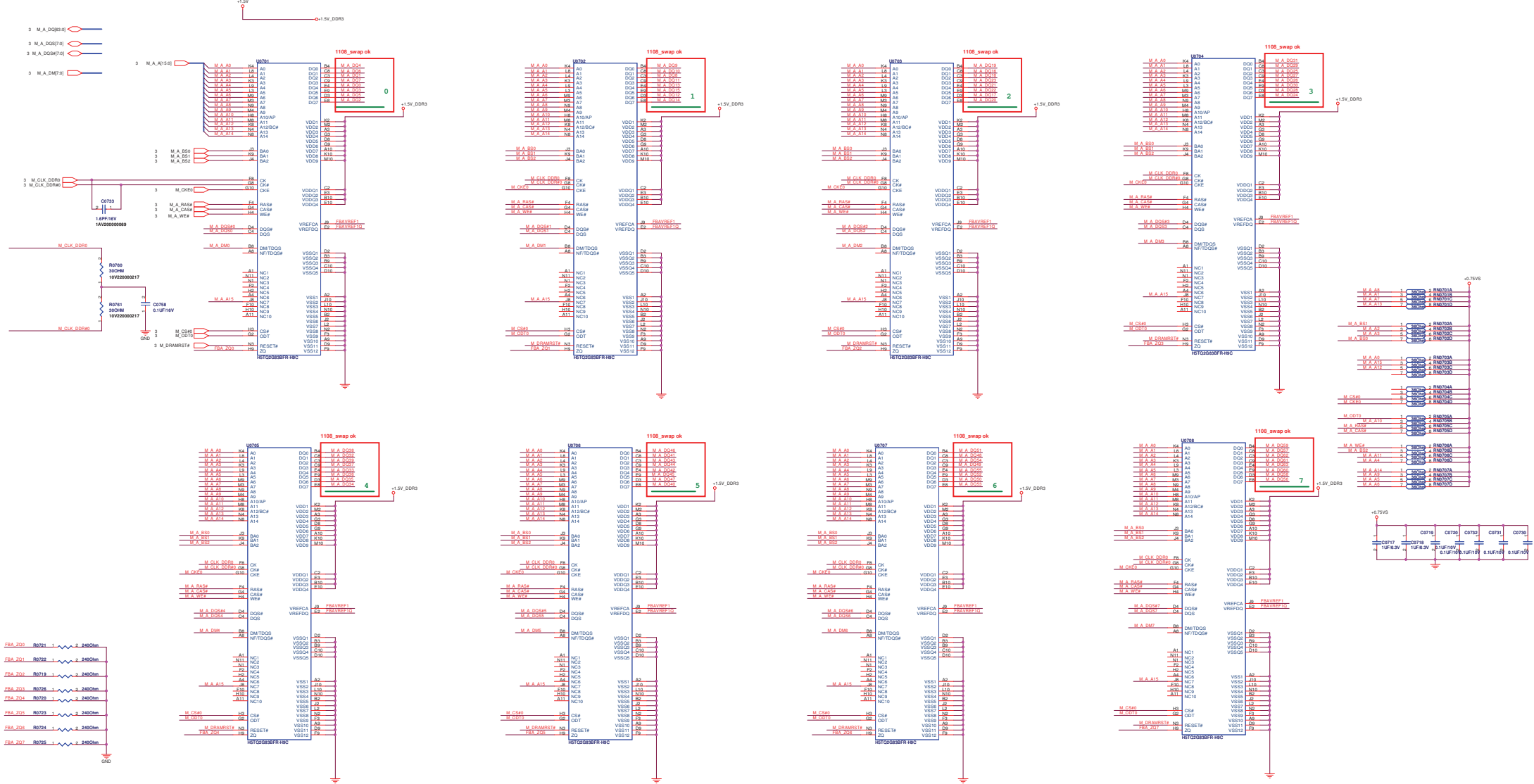
+V CORE
 10UF x 7
 1UF x 4
 0.1UF x 5
 180PF x 2

+VDDCR_NB
 10UF x 7
 1UF x 4
 0.1UF x 5
 180PF x 2

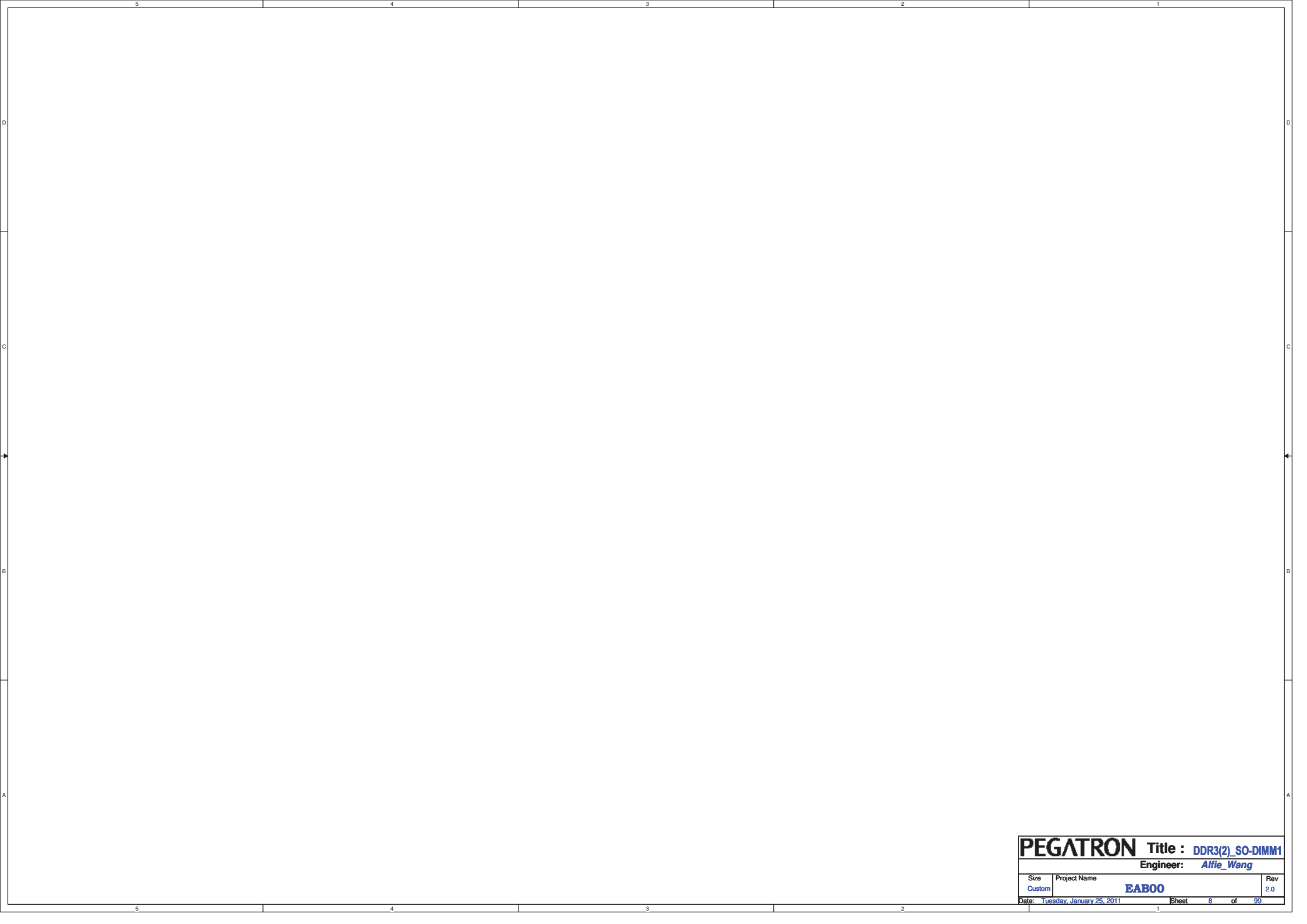




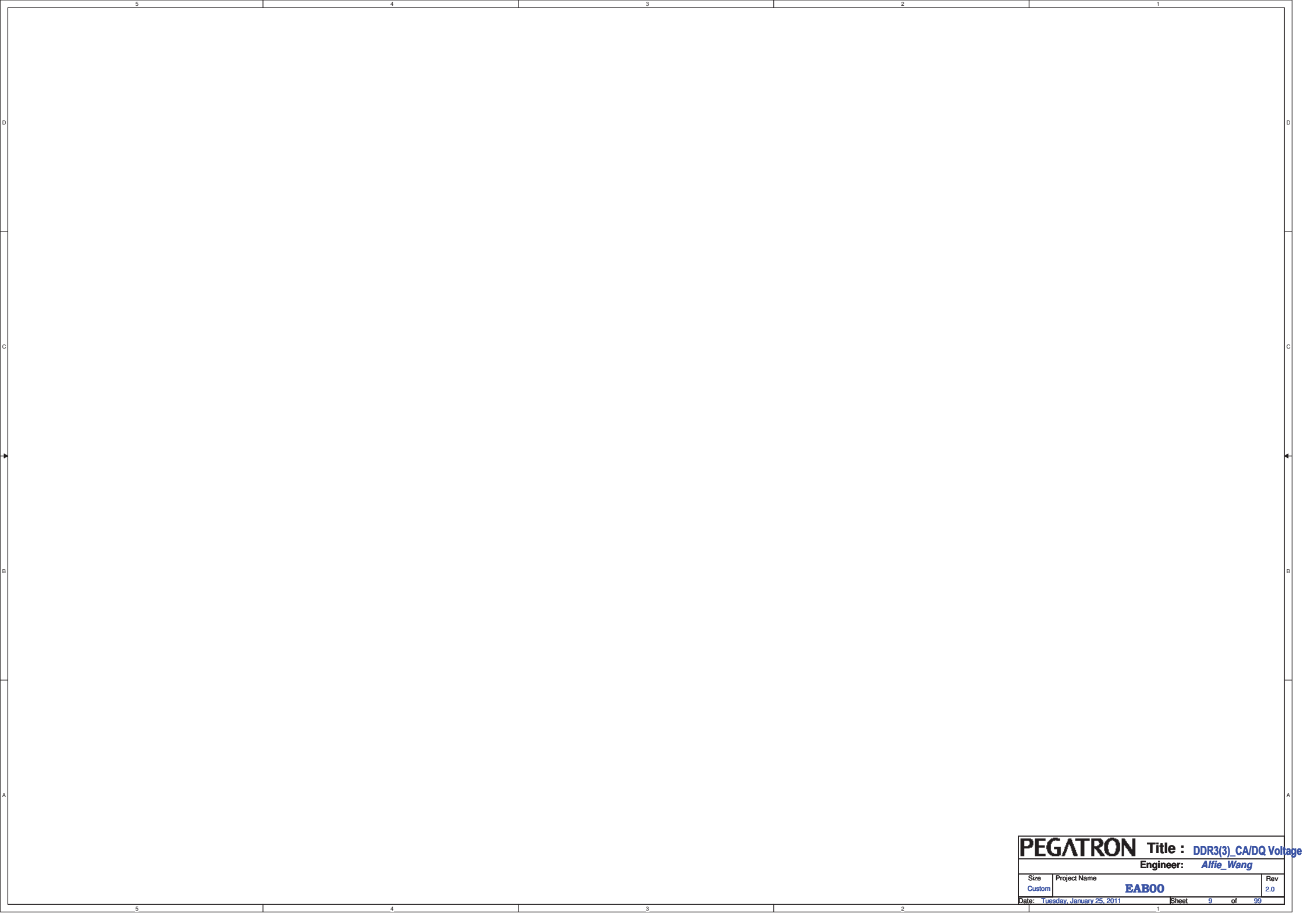
PEGATRON		Title : CPU(4)_PWR	
		Engineer: Alfie_Wang	
Size	Project Name		Rev
Custom	EABOO		2.0
Date: Tuesday, January 25, 2011		Sheet	6 of 99



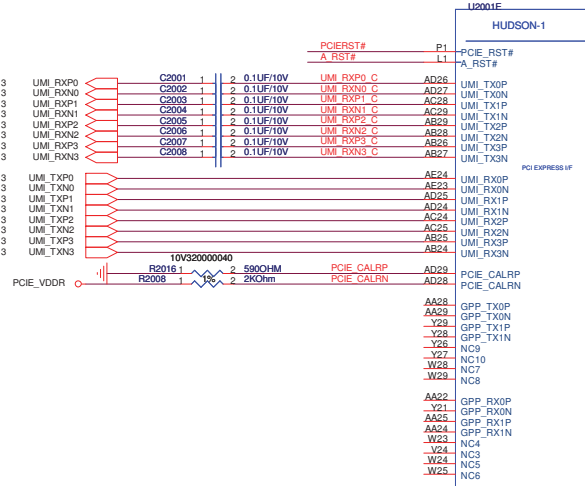
0107 Remove SPD



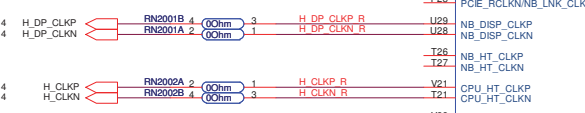
PEGATRON		Title : DDR3(2)_SO-DIMM1	
		Engineer: <i>Alfie_Wang</i>	
Size	Project Name	Rev	
Custom	EAB00	2.0	
Date: <i>Tuesday, January 25, 2011</i>		Sheet	6 of 99



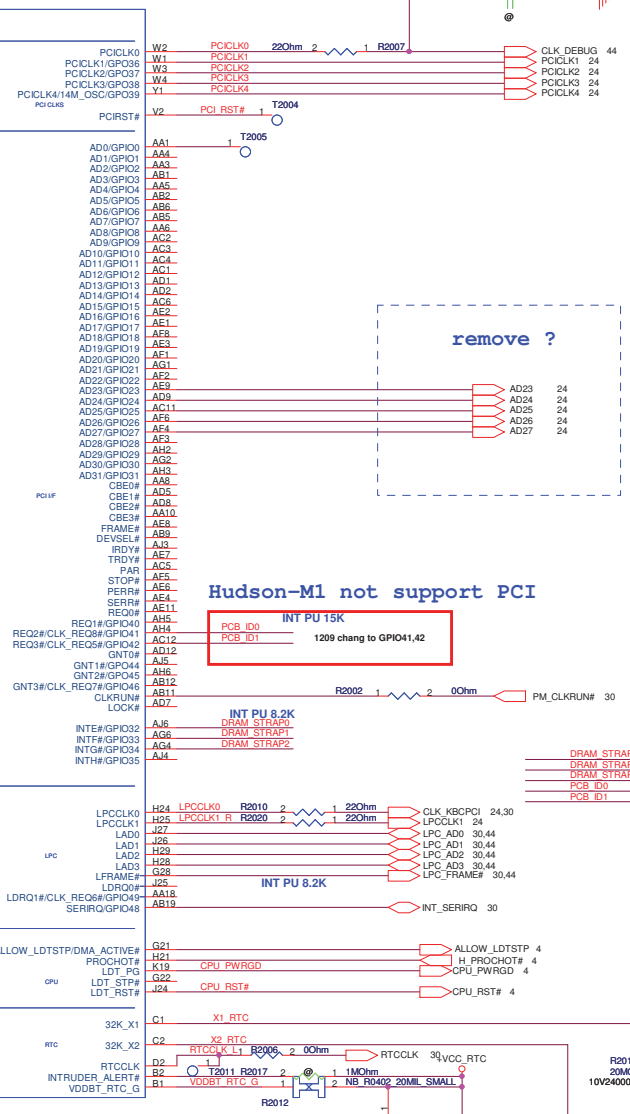
PEGATRON		Title : DDR3(3)_CA/DQ Voltage	
		Engineer: Alfie_Wang	
Size	Project Name	Rev	
Custom	EAB00	2.0	
Date: <u>Tuesday, January 25, 2011</u>		Sheet	9 of 99



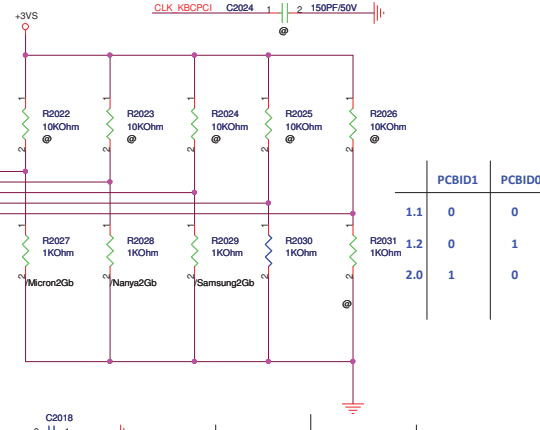
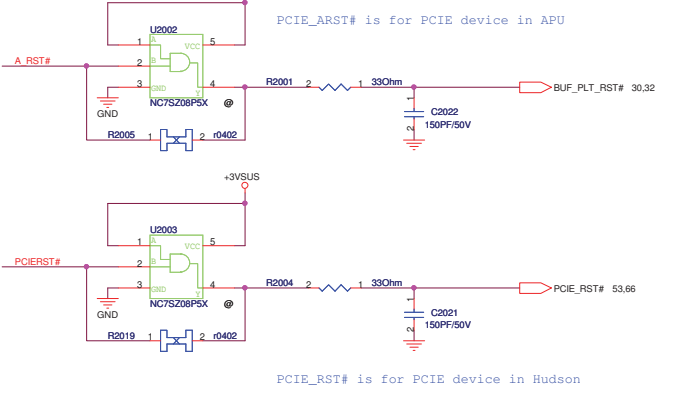
For internal clock generator mode:
NB_LNK_CLKP. Not used. Left unconnected



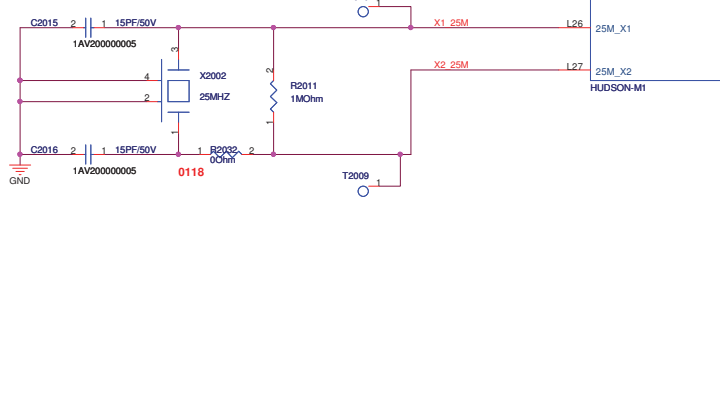
1204 remove PCIE CR



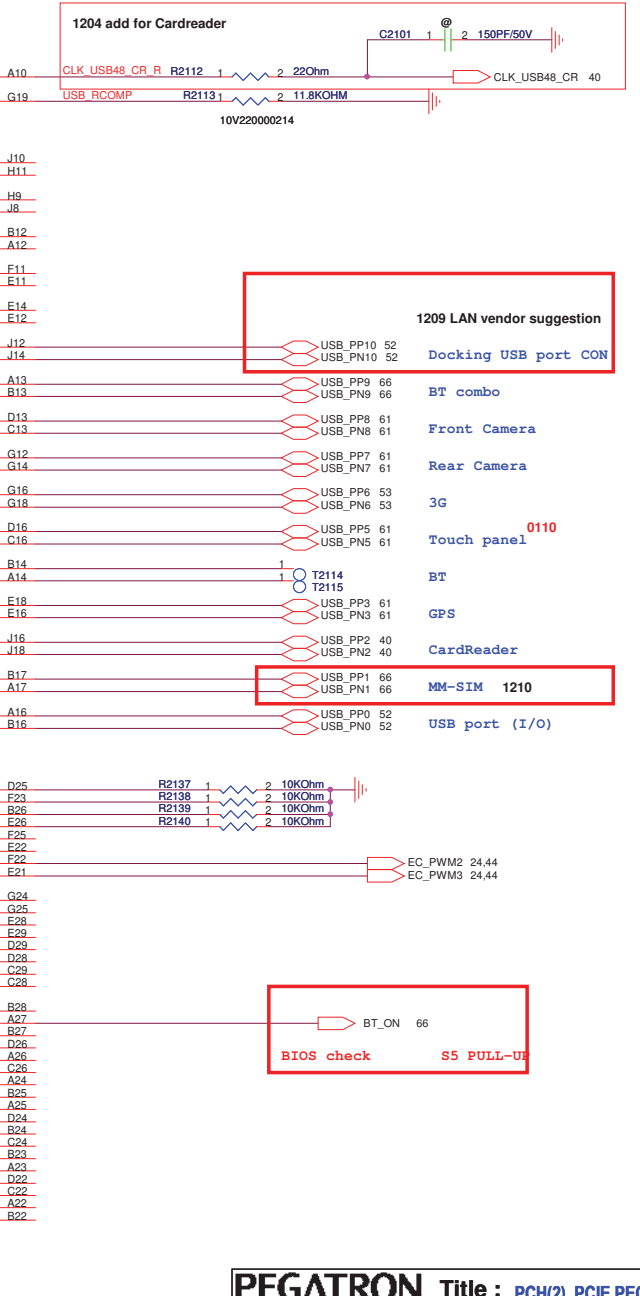
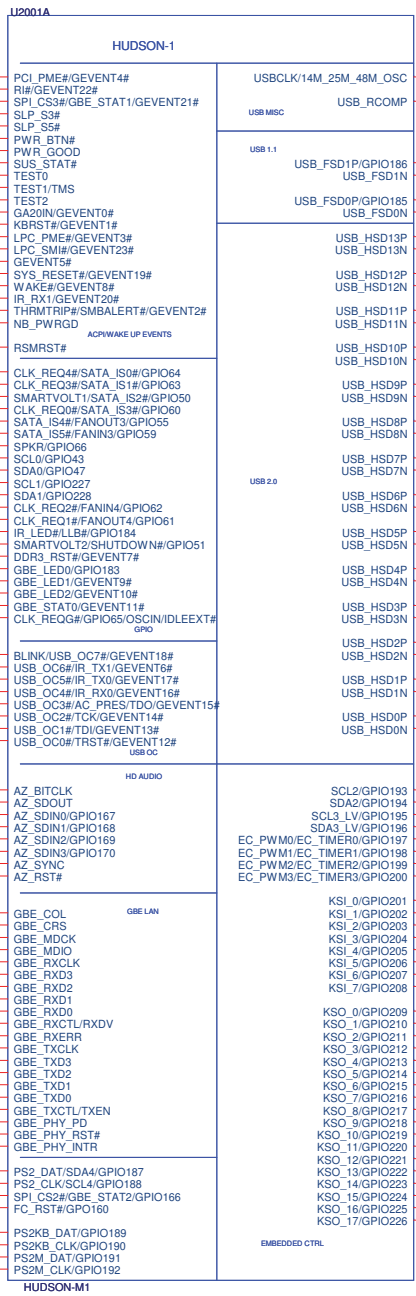
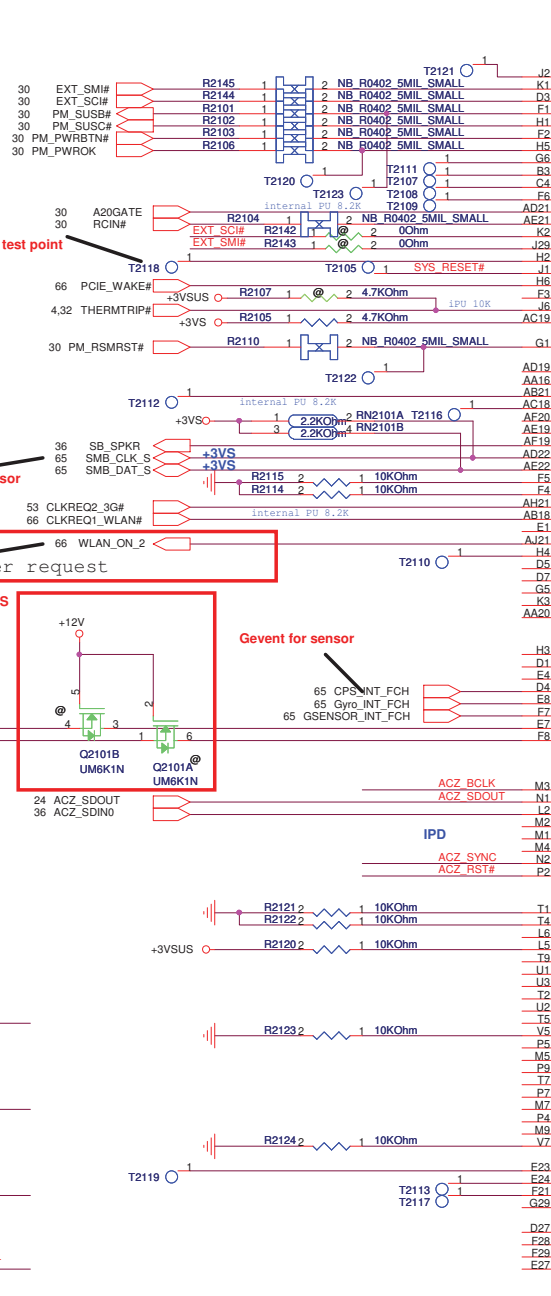
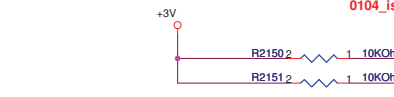
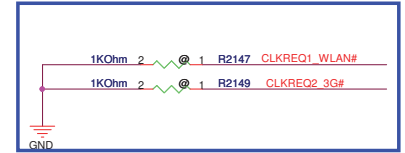
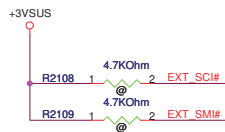
Hudson-M1 not support PCI



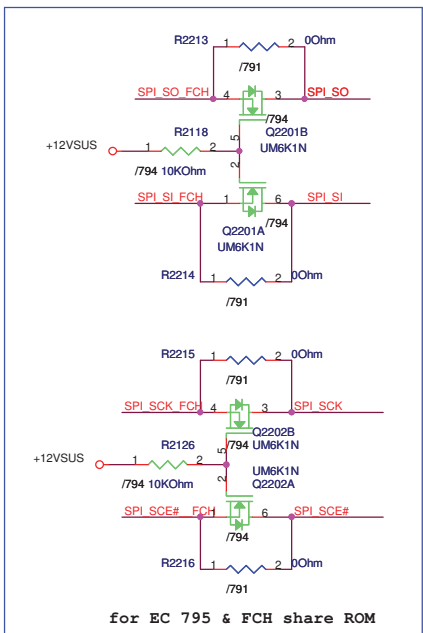
	DRAM_STRAP0	DRAM_STRAP1	DRAM_STRAP3
Hynix(2Gb) default	1	1	1
Micron(2Gb)	0	1	1
Nanya(2Gb)	1	0	1
Samsung(2Gb)	1	1	0



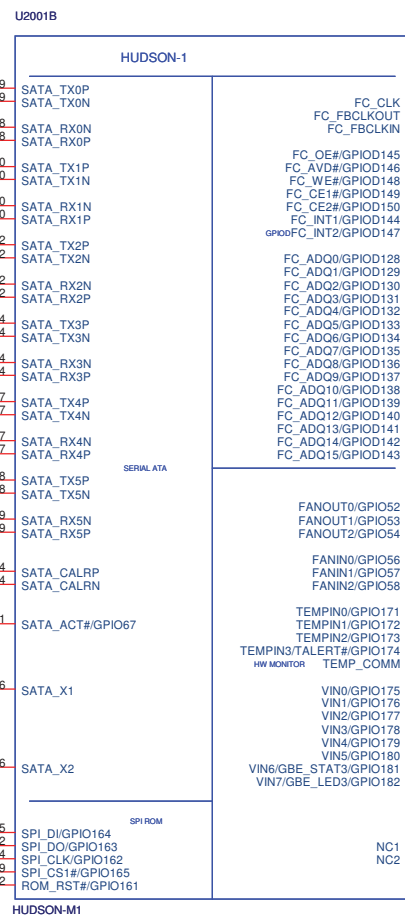
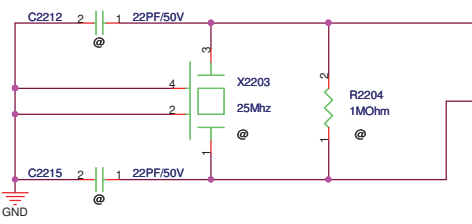
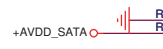
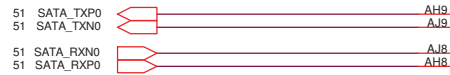
CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



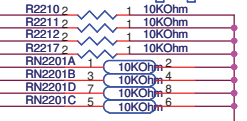
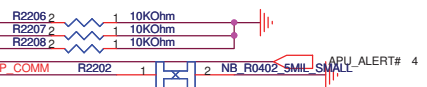
Hudson-M1 not support MAC and PS2

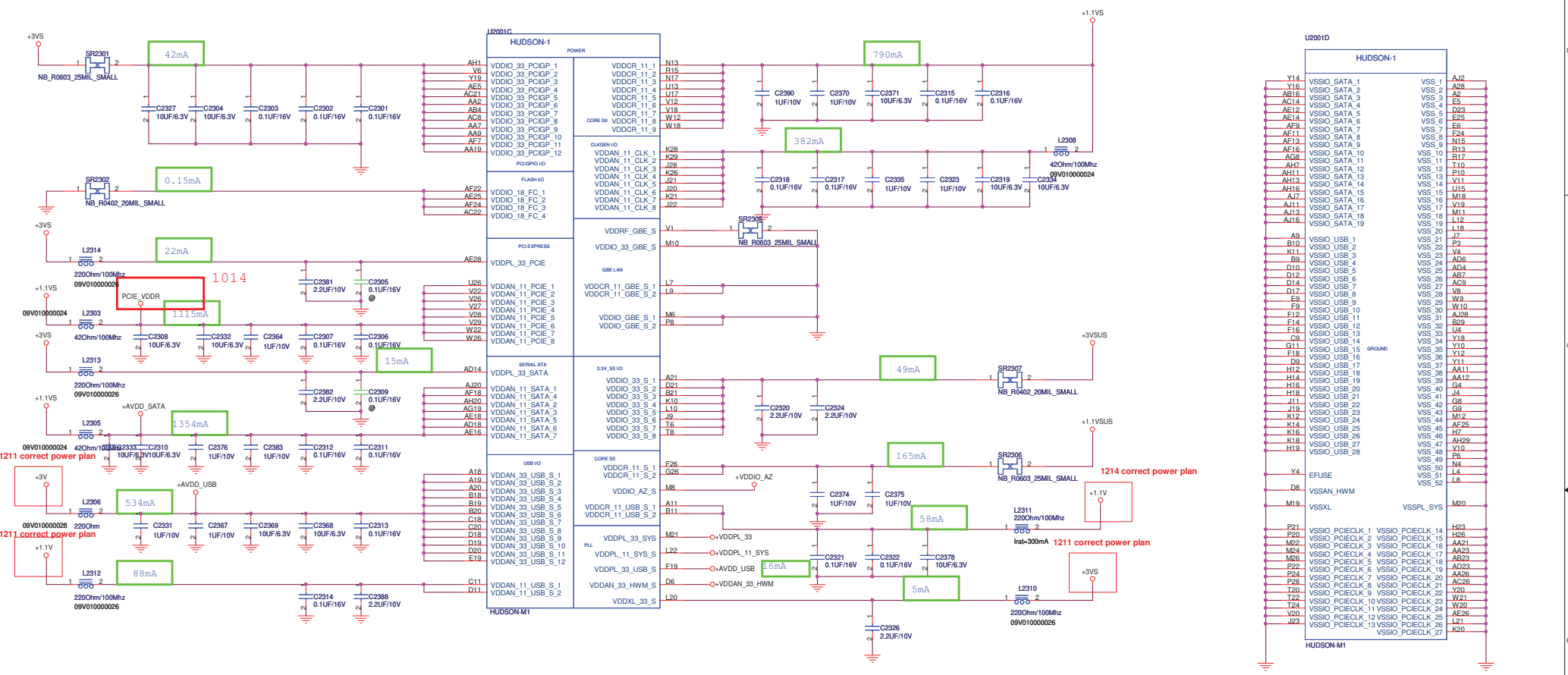


SSD

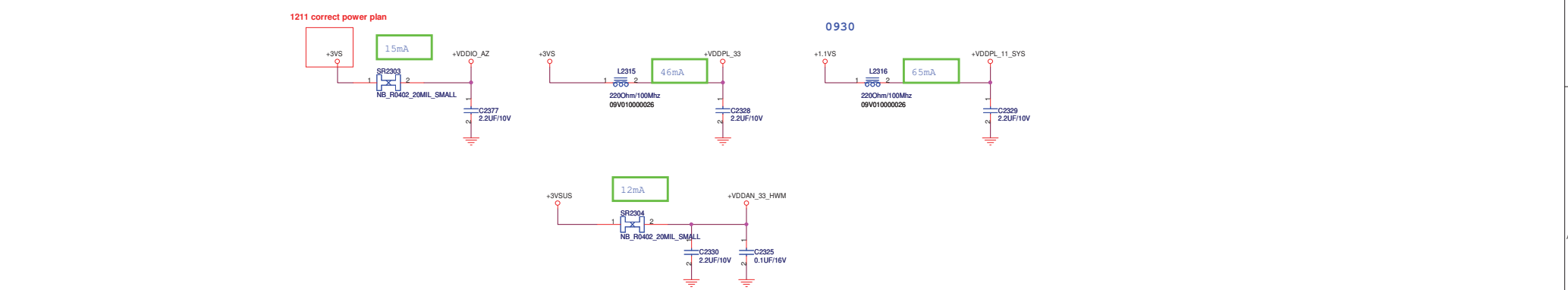


Hudson-M1 not support flash memory

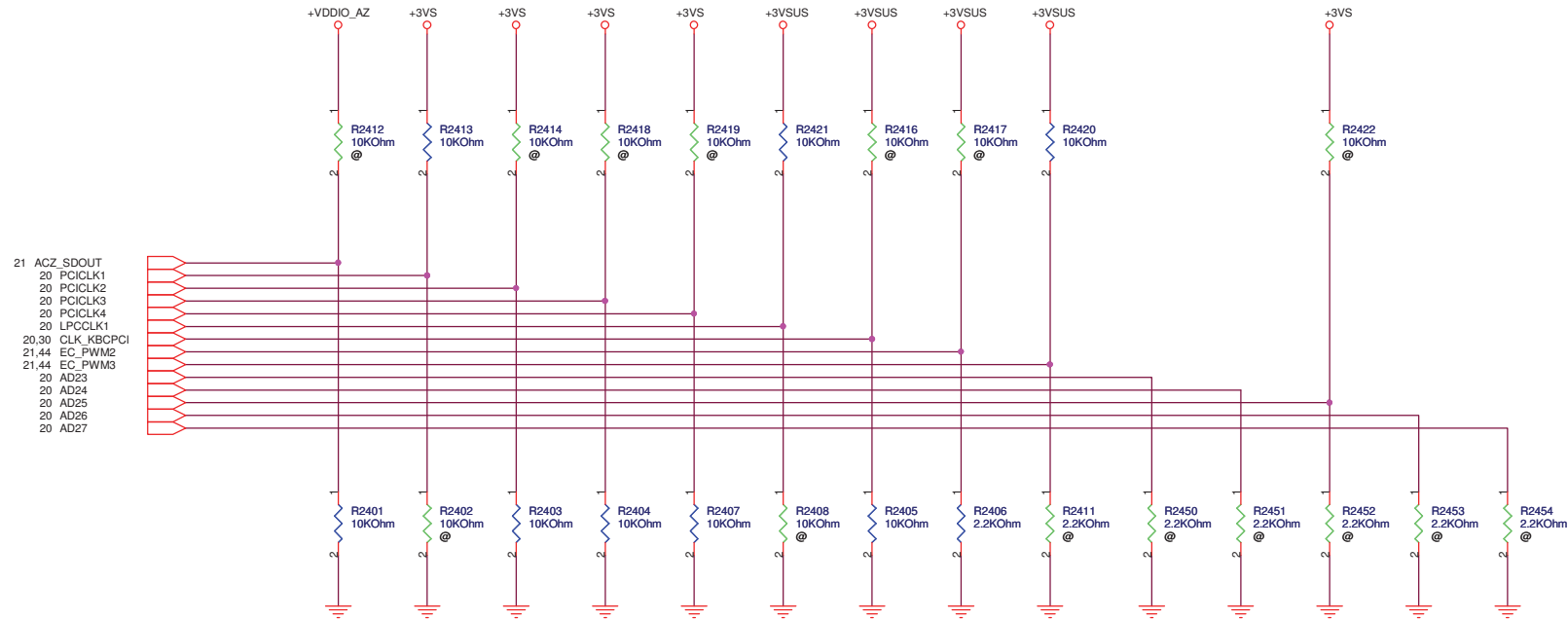




U2001D		
HUDSON-1		
Y14	VSSIO SATA_1	VSS_1 AJ2
Y16	VSSIO SATA_2	VSS_2 A28
AB16	VSSIO SATA_3	VSS_3 A2
AC14	VSSIO SATA_4	VSS_4 E5
AE14	VSSIO SATA_5	VSS_5 D23
AF0	VSSIO SATA_6	VSS_6 E5
AF2	VSSIO SATA_7	VSS_7 E6
AE11	VSSIO SATA_8	VSS_8 M15
AE13	VSSIO SATA_9	VSS_9 F24
AE16	VSSIO SATA_10	VSS_10 R13
AG8	VSSIO SATA_11	VSS_11 T10
AH7	VSSIO SATA_12	VSS_12 P10
AH13	VSSIO SATA_13	VSS_13 P10
AH16	VSSIO SATA_14	VSS_14 U15
AJ7	VSSIO SATA_15	VSS_15 V19
AJ7	VSSIO SATA_16	VSS_16 M18
AJ11	VSSIO SATA_17	VSS_17 V19
AJ13	VSSIO SATA_18	VSS_18 M11
AJ16	VSSIO SATA_19	VSS_19 L12
A9	VSSIO USB_1	VSS_20 L18
R10	VSSIO USB_2	VSS_21 J7
K11	VSSIO USB_3	VSS_22 P3
B9	VSSIO USB_4	VSS_23 V4
D10	VSSIO USB_5	VSS_24 AD6
D12	VSSIO USB_6	VSS_25 AD4
D14	VSSIO USB_7	VSS_26 AC9
D17	VSSIO USB_8	VSS_27 V8
E9	VSSIO USB_9	VSS_28 W9
F9	VSSIO USB_10	VSS_29 W10
F14	VSSIO USB_11	VSS_30 B29
F16	VSSIO USB_12	VSS_31 U4
G11	VSSIO USB_13	VSS_32 Y18
H12	VSSIO USB_14	VSS_33 Y10
H16	VSSIO USB_15	VSS_34 Y12
H18	VSSIO USB_16	VSS_35 Y11
H19	VSSIO USB_17	VSS_36 AA12
H21	VSSIO USB_18	VSS_37 J4
H24	VSSIO USB_19	VSS_38 J4
H26	VSSIO USB_20	VSS_39 G8
H28	VSSIO USB_21	VSS_40 M12
H31	VSSIO USB_22	VSS_41 G9
H32	VSSIO USB_23	VSS_42 M12
H34	VSSIO USB_24	VSS_43 AF25
H36	VSSIO USB_25	VSS_44 H17
H38	VSSIO USB_26	VSS_45 AH29
H39	VSSIO USB_27	VSS_46 V10
D9	VSSIO USB_28	VSS_47 F9
D9	VSSIO USB_29	VSS_48 N4
Y4	EFUSE	VSS_49 L4
Y8	VSSAN_HWM	VSS_50 L4
M19	VSSXL	VSS_51 M20
P21	VSSIO_PCIECLK_1	VSSIO_PCIECLK_14 H23
P20	VSSIO_PCIECLK_2	VSSIO_PCIECLK_15 H26
M22	VSSIO_PCIECLK_3	VSSIO_PCIECLK_16 A21
M24	VSSIO_PCIECLK_4	VSSIO_PCIECLK_17 A22
M26	VSSIO_PCIECLK_5	VSSIO_PCIECLK_18 AB23
P22	VSSIO_PCIECLK_6	VSSIO_PCIECLK_19 A23
P24	VSSIO_PCIECLK_7	VSSIO_PCIECLK_20 A26
P26	VSSIO_PCIECLK_8	VSSIO_PCIECLK_21 AC26
T20	VSSIO_PCIECLK_9	VSSIO_PCIECLK_22 Y20
T22	VSSIO_PCIECLK_10	VSSIO_PCIECLK_23 W21
T24	VSSIO_PCIECLK_11	VSSIO_PCIECLK_24 W20
V20	VSSIO_PCIECLK_12	VSSIO_PCIECLK_25 AE26
V22	VSSIO_PCIECLK_13	VSSIO_PCIECLK_26 L21
V23	VSSIO_PCIECLK_14	VSSIO_PCIECLK_27 K20



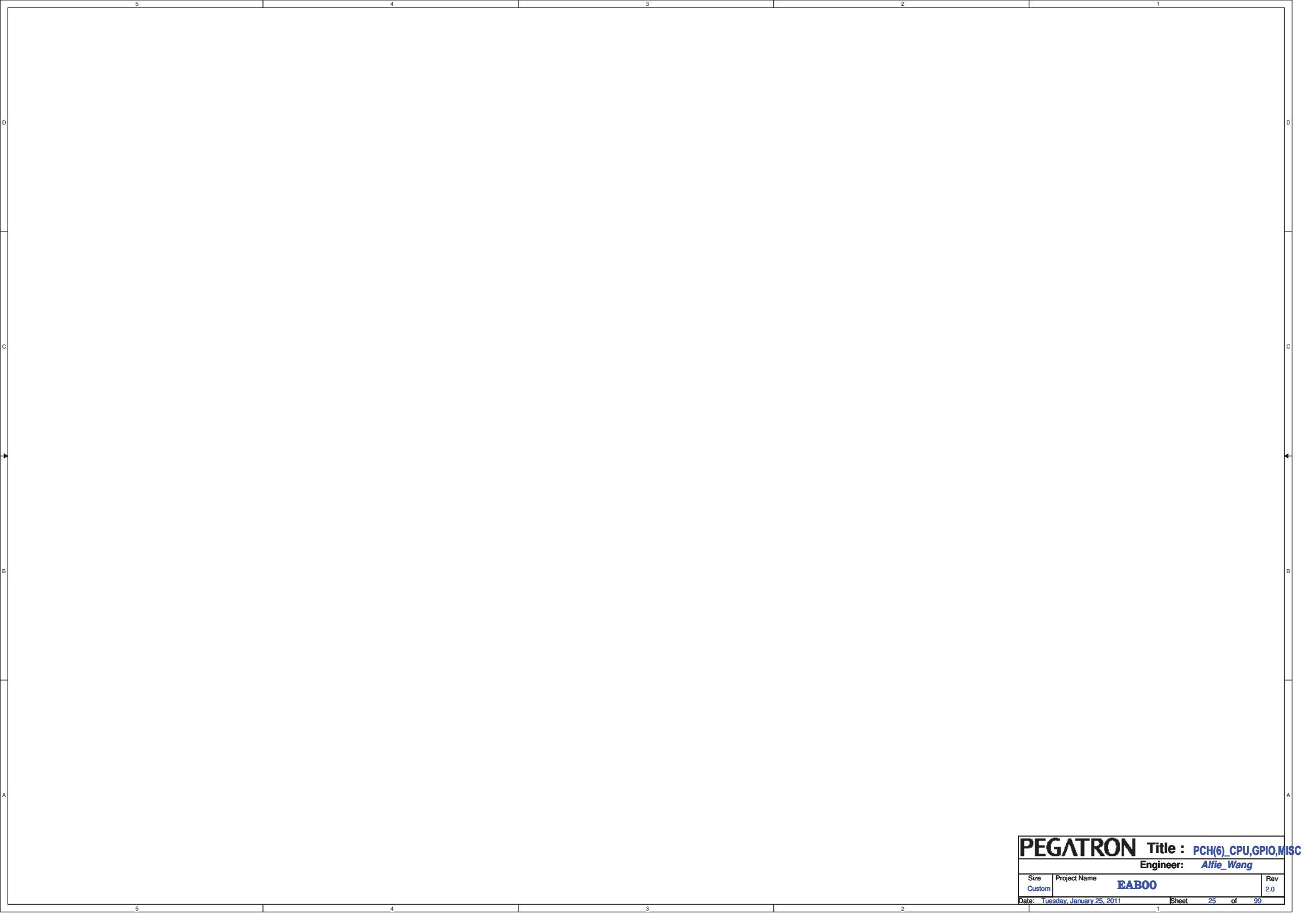
Strap Pins



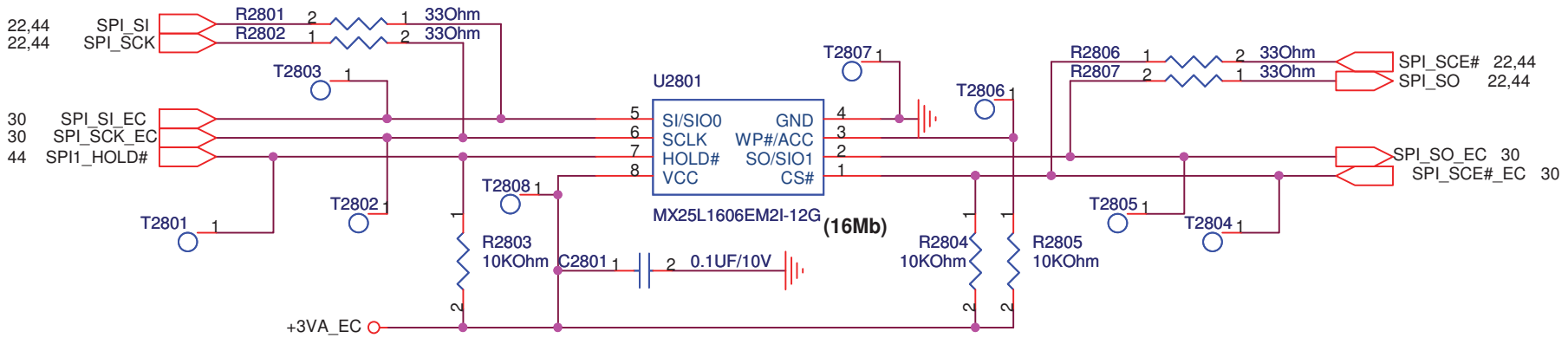
	ACZ_SDOUT_AUD	PCICLK1	PCICLK2	PCICLK3	PCICLK4	LPCCLK0 CLK_KBCPCI	LPCCLK1	EC_PWM2	EC_PWM3	
High	low power mode	PCIE Gen2	watchdog timer enable	debug	no-Fusion clock mode	EC enable	clock gen. enable	H	L	LPC ROM
Low	performance mode	PCIE Gen1	watchdog timer disable	ignore debug	Fusion clock mode	EC disable	clock gen. disable	L	H	SPI ROM

Debug Straps

	AD23	AD24	AD25	AD26	AD27
High	disable PCI mem boot	default PCIE straps	use FC PLL	disable ILA autorun	use PCI PLL
Low	enable PCI mem boot	EEPROM PCIE straps	bypass FC PLL	enable ILA autorun	by pass PCI PLL



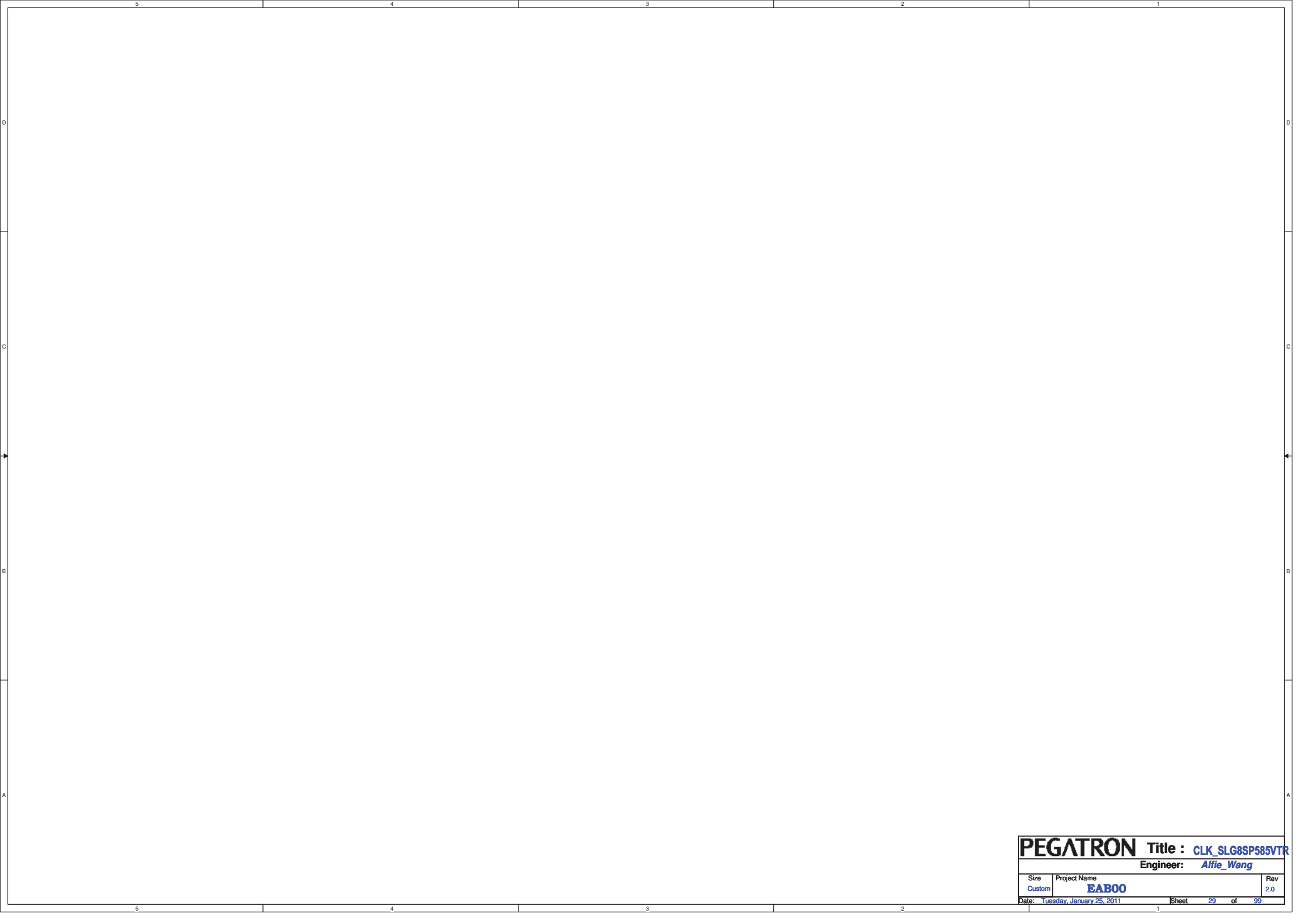
PEGATRON		Title : PCH(6)_CPU,GPIO,MISC	
		Engineer: Alfie_Wang	
Size Custom	Project Name EAB00	Rev 2.0	
Date: Tuesday, January 25, 2011		Sheet	25 of 99



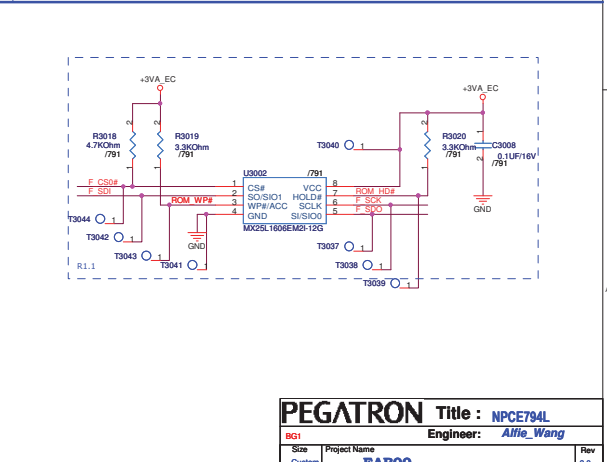
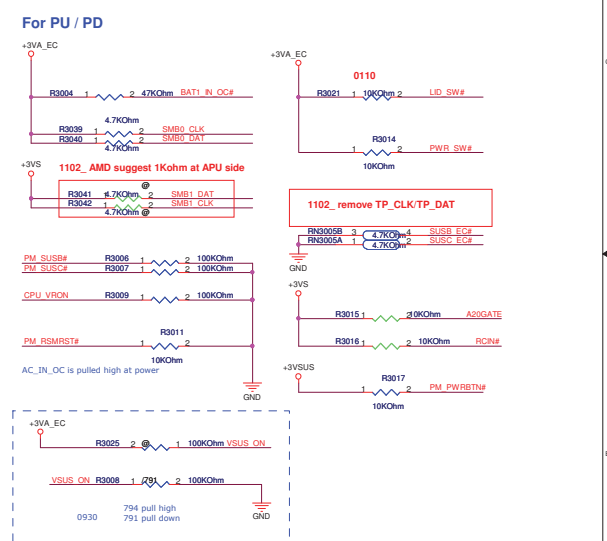
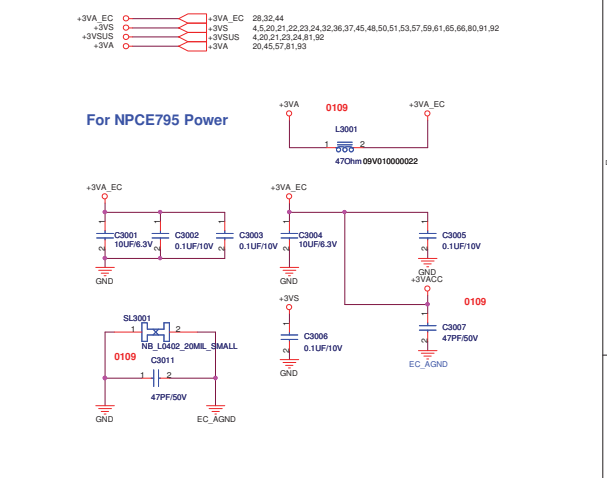
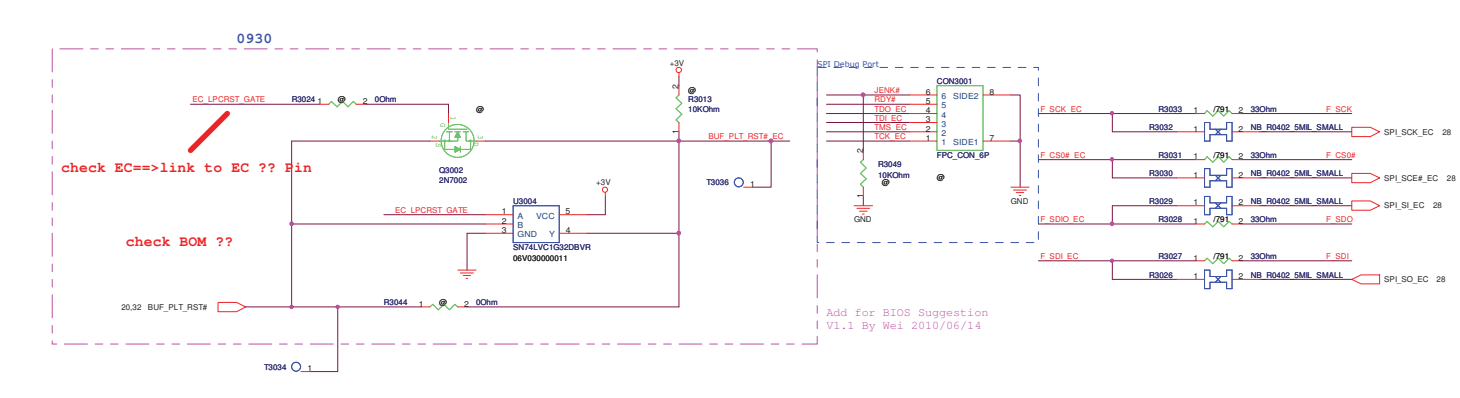
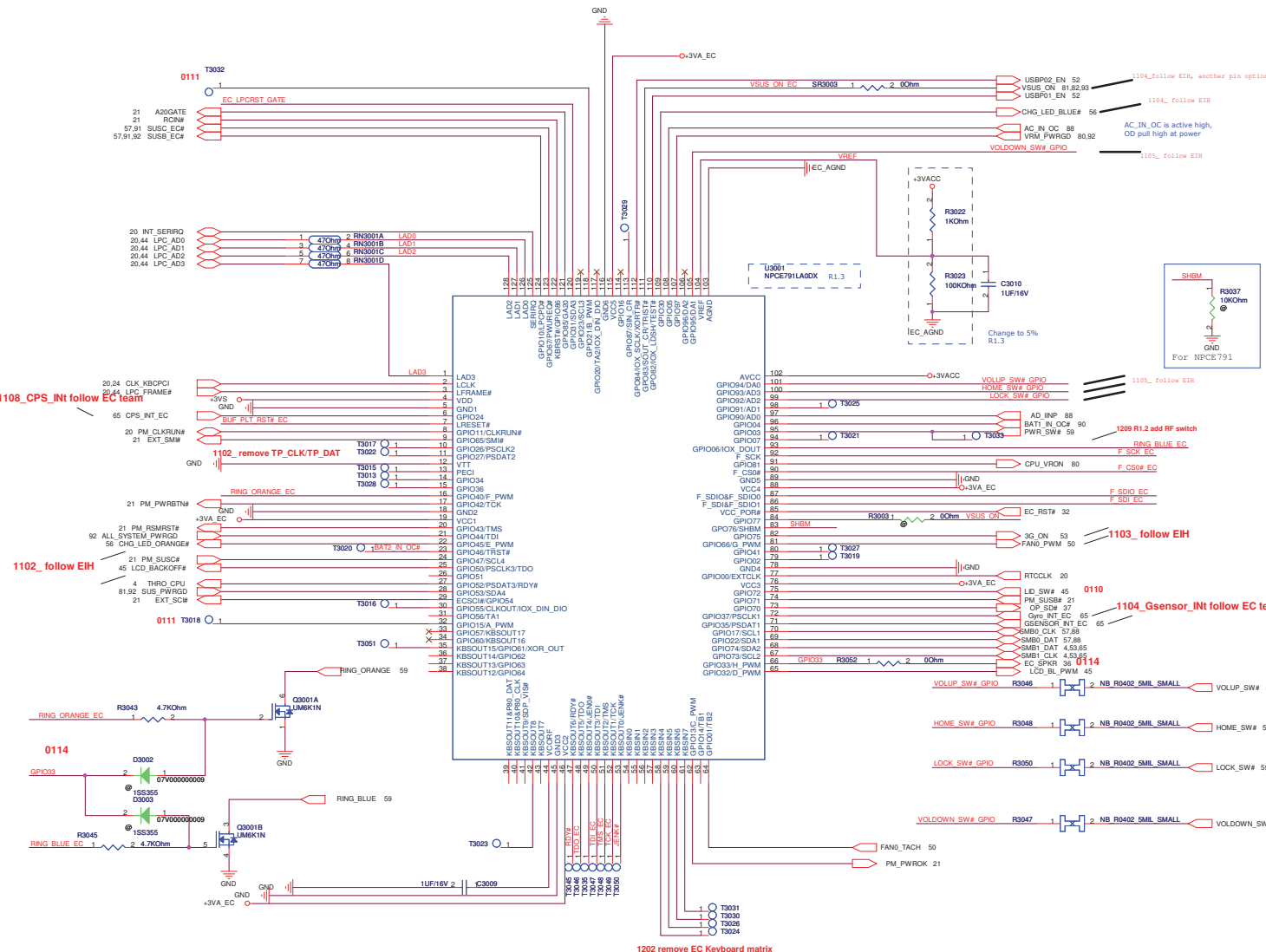
WINBOND:0500-00P4000
 MXIC: 0500-00TY000

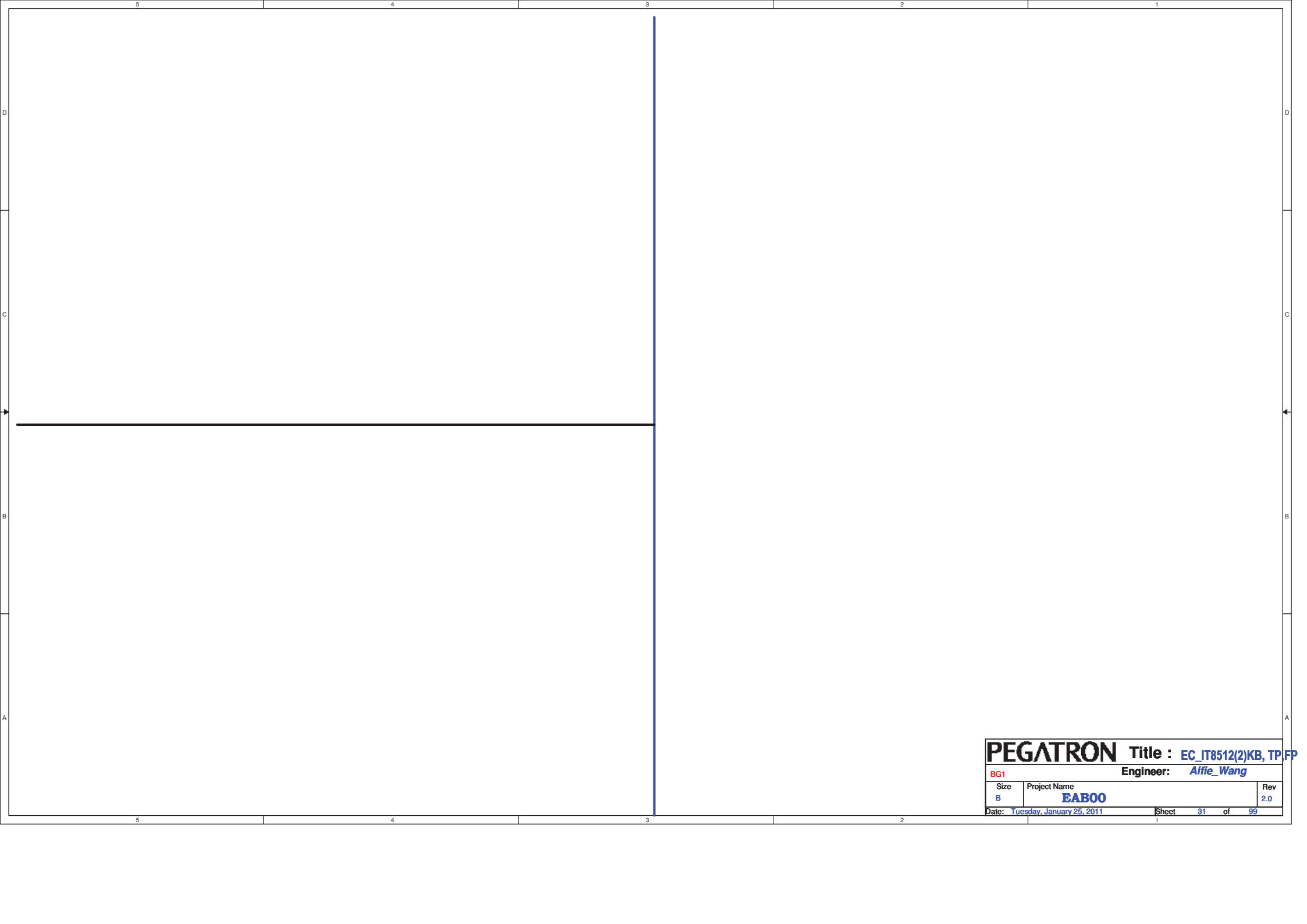
reserved for BIOS testing

Title		
SPI_ROM		
Size	Document Number	Rev
A	EAB00	2.0
Date:	Tuesday, January 25, 2011	Sheet 28 of 1



PEGATRON		Title : CLK_SLG8SP585VTR	
		Engineer: Alfie_Wang	
Size	Project Name		Rev
Custom	EAB00		2.0
Date: Tuesday, January 25, 2011		Sheet	29 of 99





PEGATRON Title : EC_IT8512(2)KB, TPFP

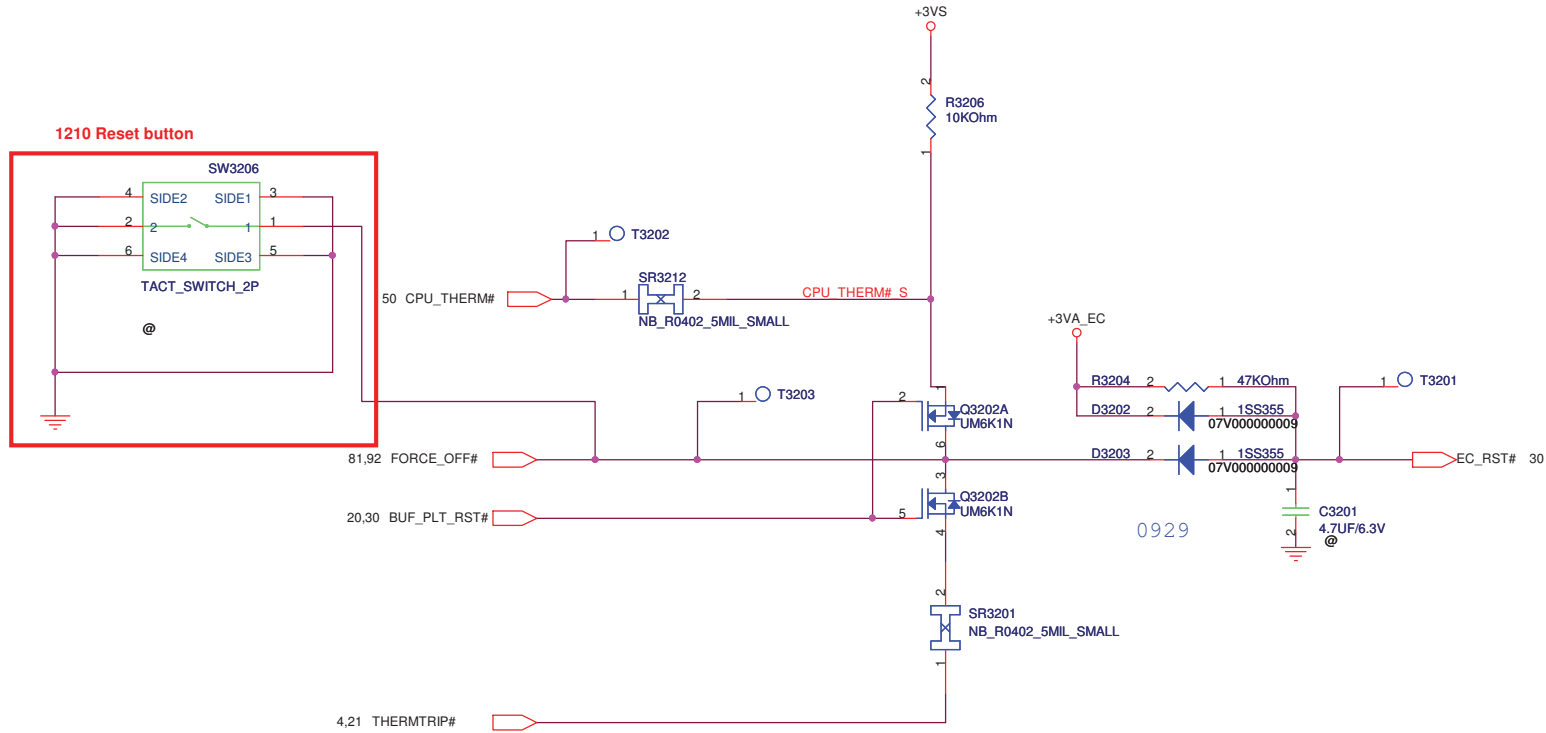
BG1 Engineer: *Alfie_Wang*

Size	Project Name	Rev
B	EABOO	2.0

Date: Tuesday, January 25, 2011 Sheet 31 of 99

Thermal Policy

NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us



PEGATRON		Title : RST_Reset Circuit	
		Engineer: Alfie_Wang	
Size B	Project Name EABOO		Rev 2.0
Date: Tuesday, January 25, 2011		Sheet	32 of 99

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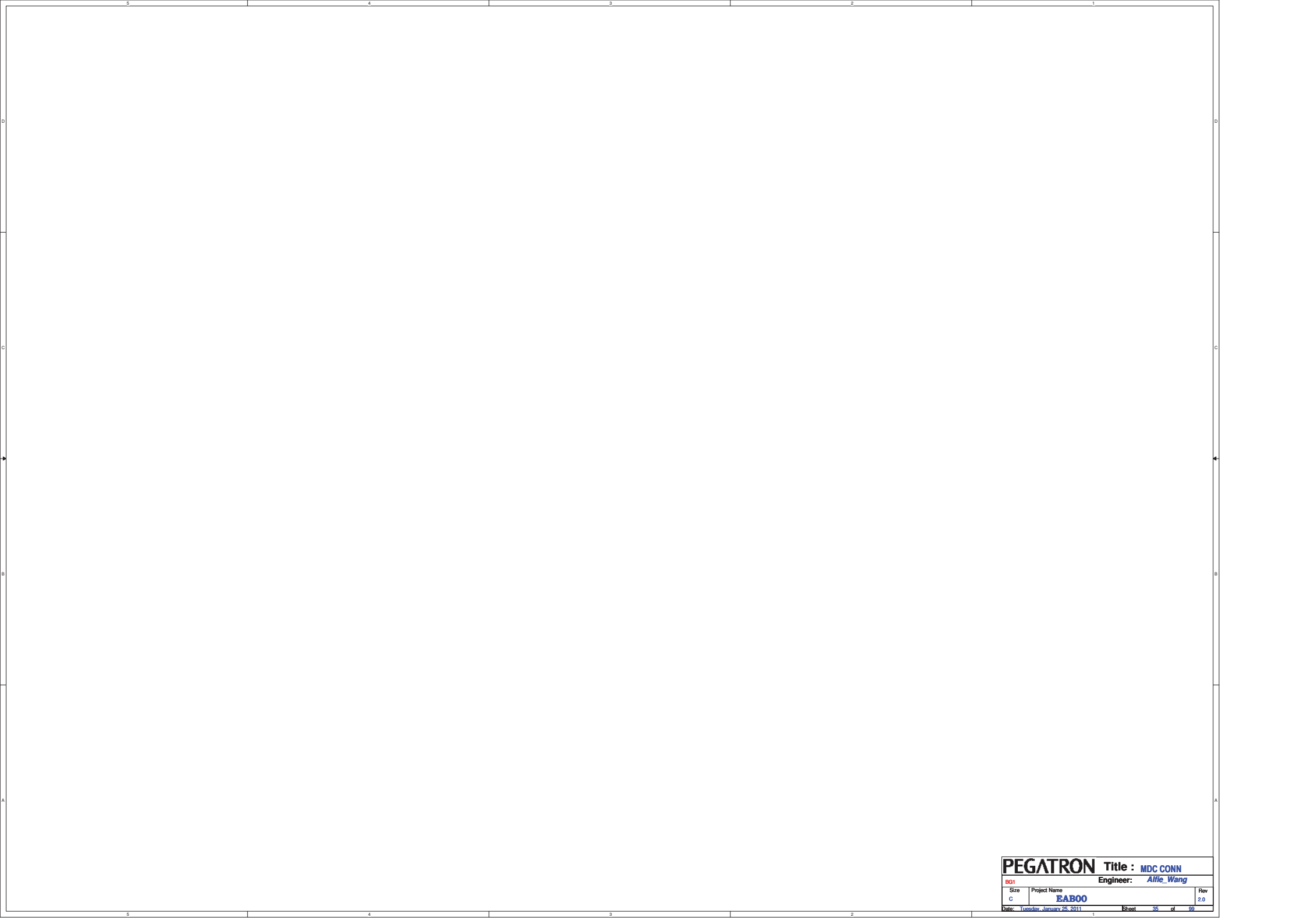
A

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PEGATRON Title :AR8151	
Engineer: <i>Alfie_Wang</i>	
Size Custom	Project Name EABOO
Date: Tuesday, January 25, 2011	Rev 2.0
Sheet 33 of 99	



PEGATRON		Title : <i>RJ45</i>	
BG1		Engineer: <i>Alfie_Wang</i>	
Size	Project Name		Rev
Custom	EABOO		2.0
Date: <i>Tuesday, January 25, 2011</i>		Sheet	34 of 99

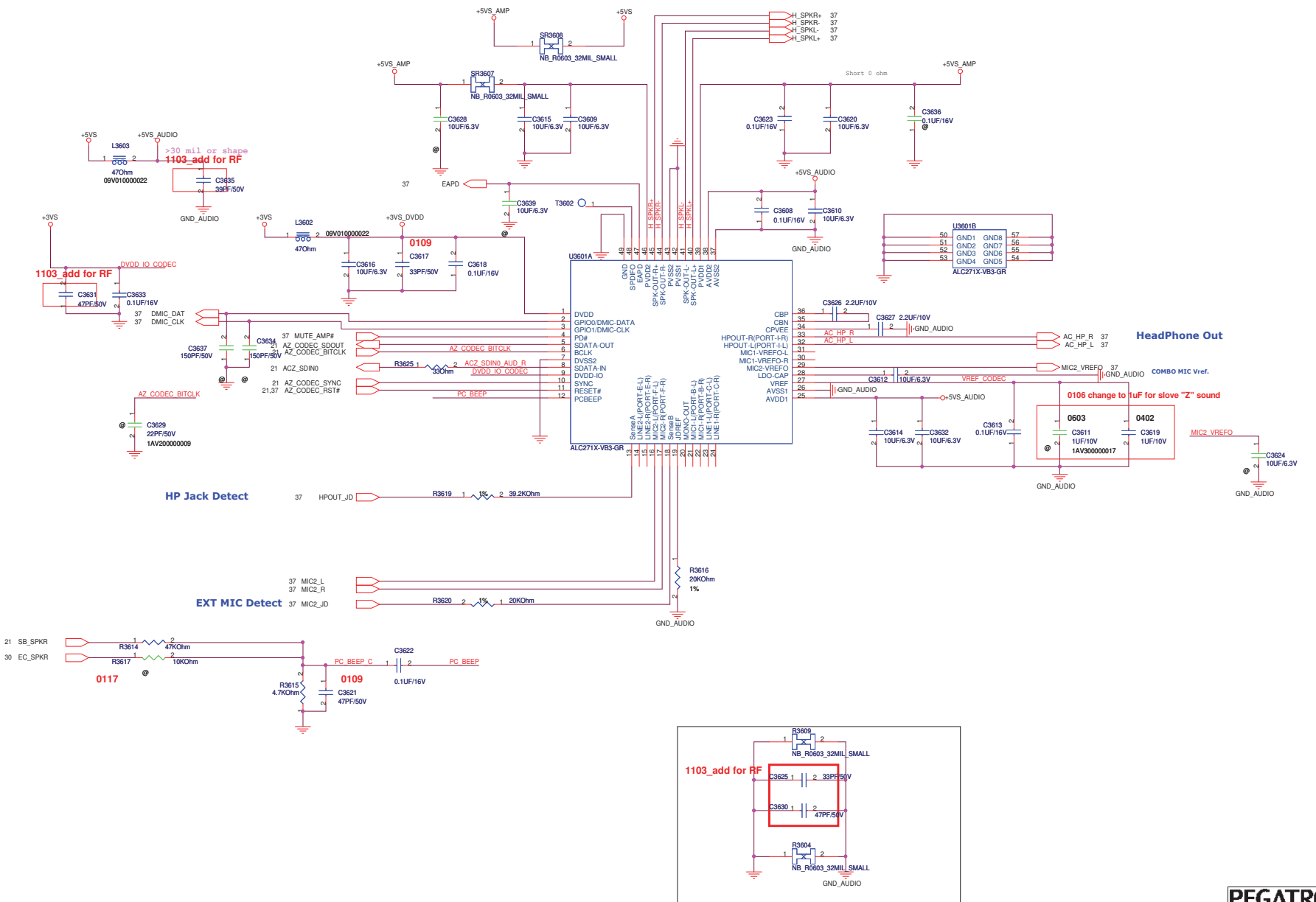
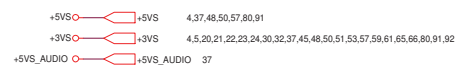


PEGATRON		Title : MDC CONN	
BG1		Engineer: <i>Ailie Wang</i>	
Size	Project Name	Rev	
C	EAB00	2.0	
Date: Tuesday, January 25, 2011		Sheet	36 of 99

Audio Codec

DIGITAL

ANALOG

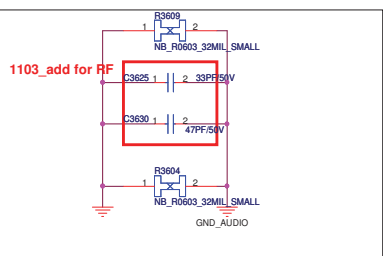


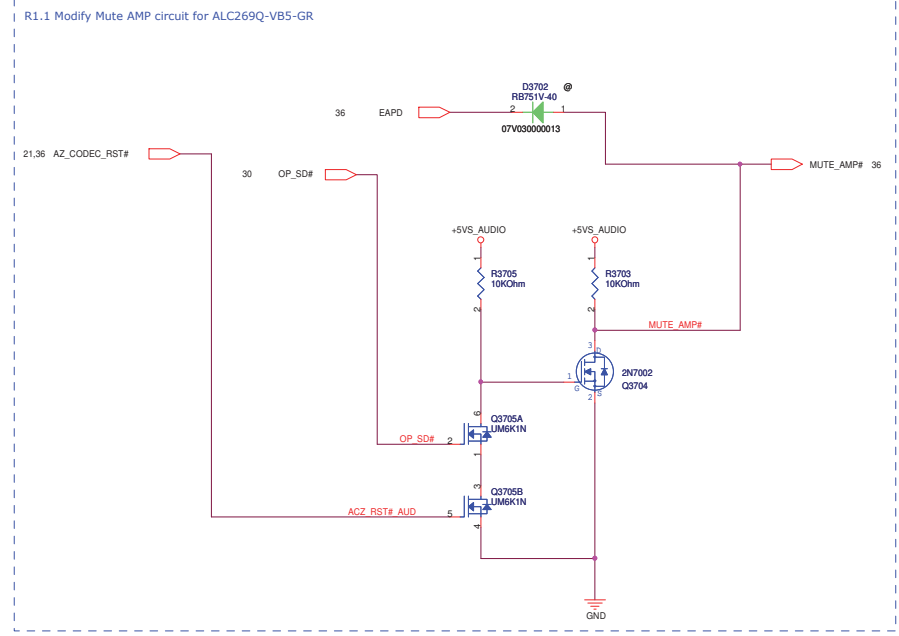
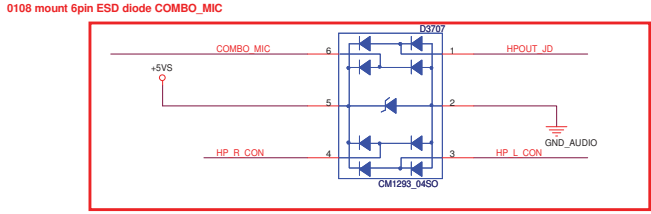
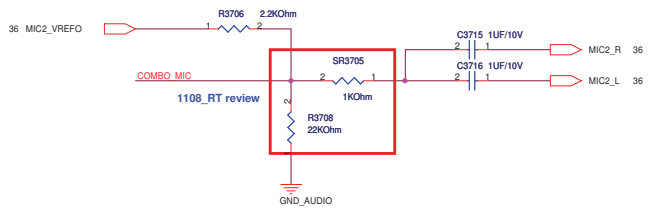
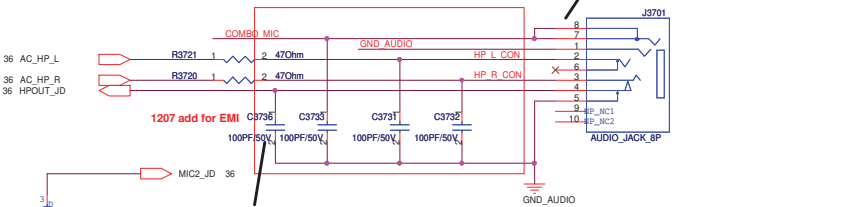
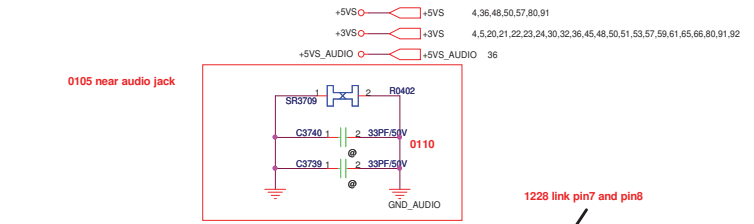
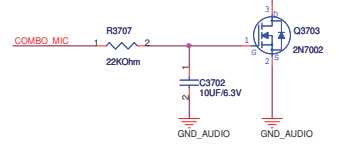
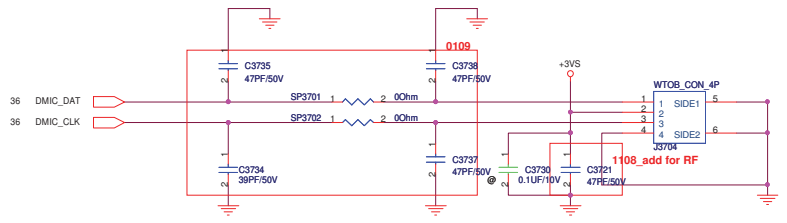
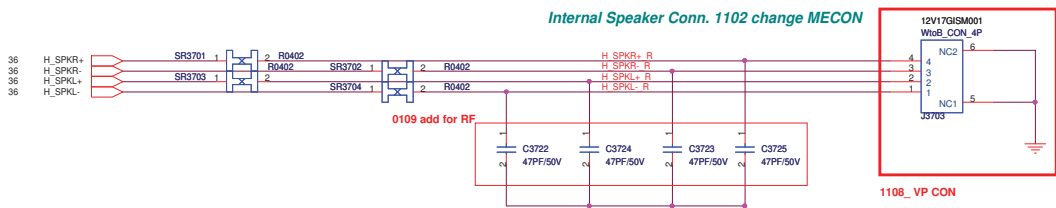
HeadPhone Out

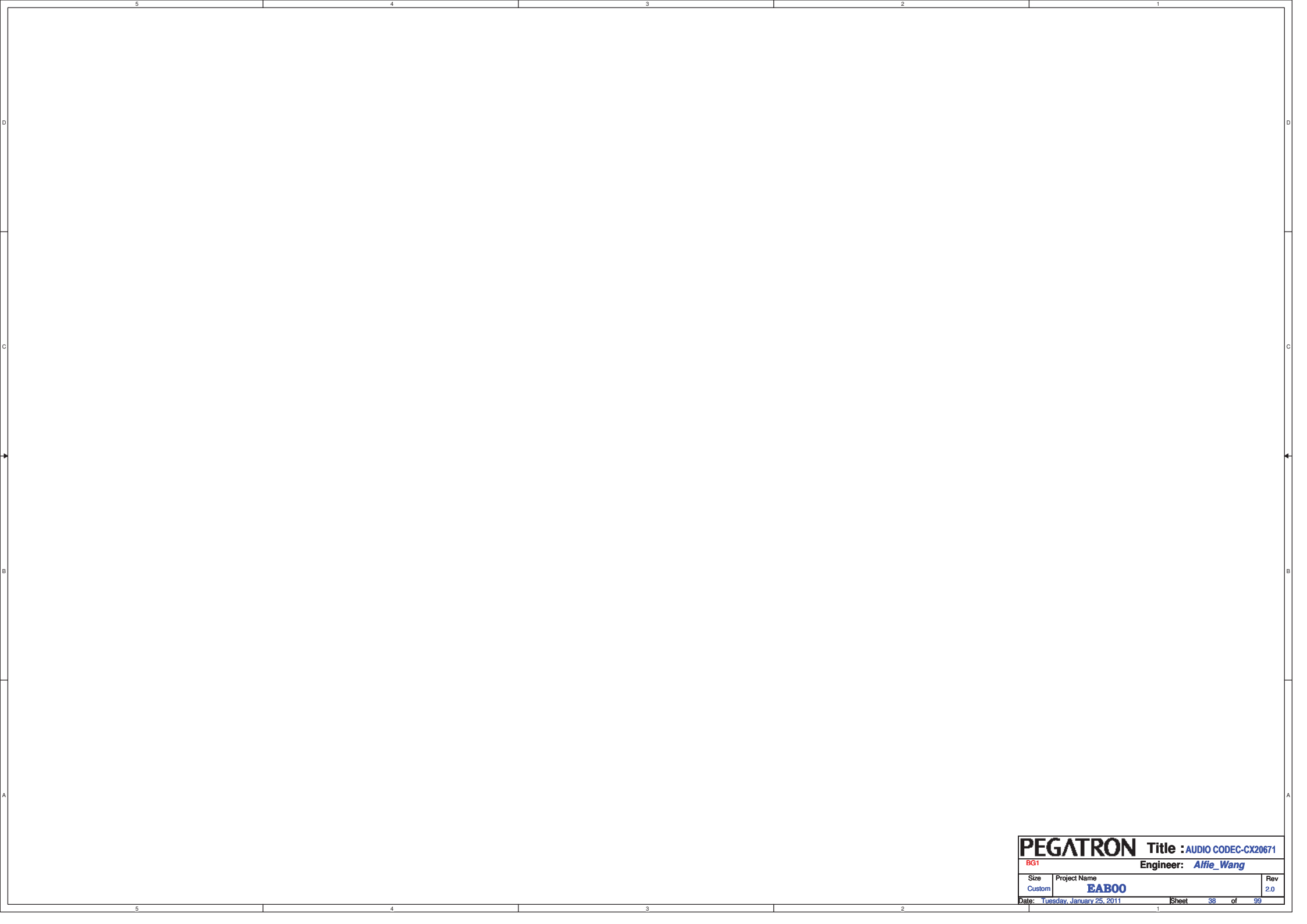
HP Jack Detect

EXT MIC Detect

MIC2 VREF







PEGATRON		Title : AUDIO CODEC-CX20671	
BG1		Engineer: Alfie_Wang	
Size	Project Name		Rev
Custom	EAB00		2.0
Date: Tuesday, January 25, 2011		Sheet	38 of 99

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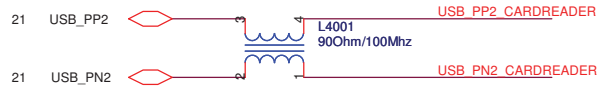
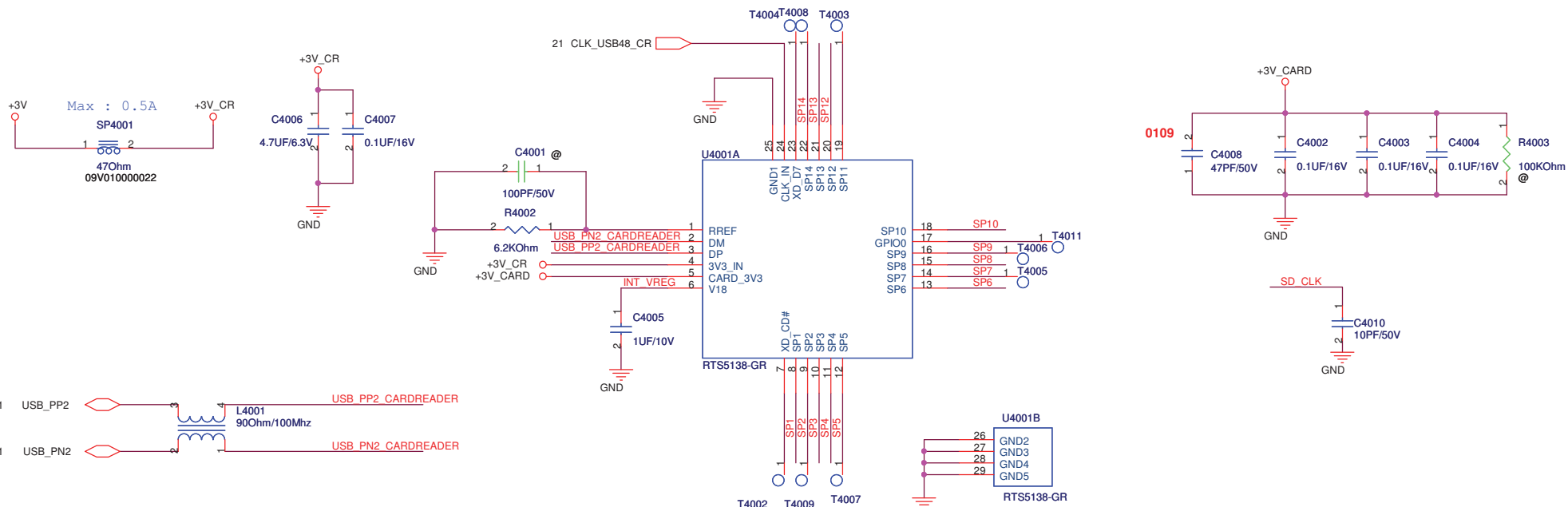
B

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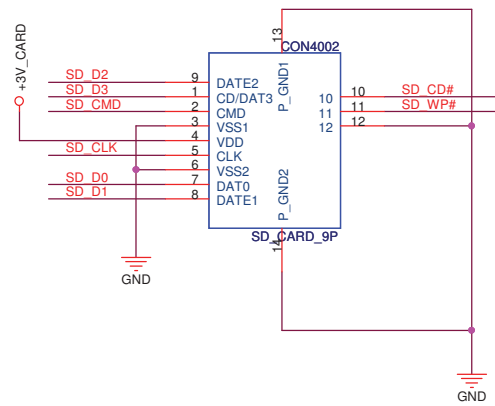
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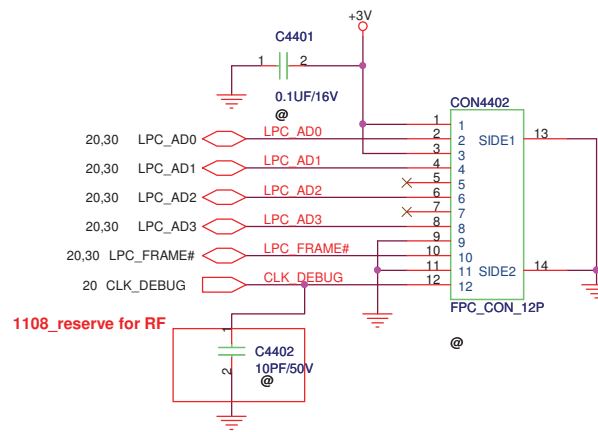
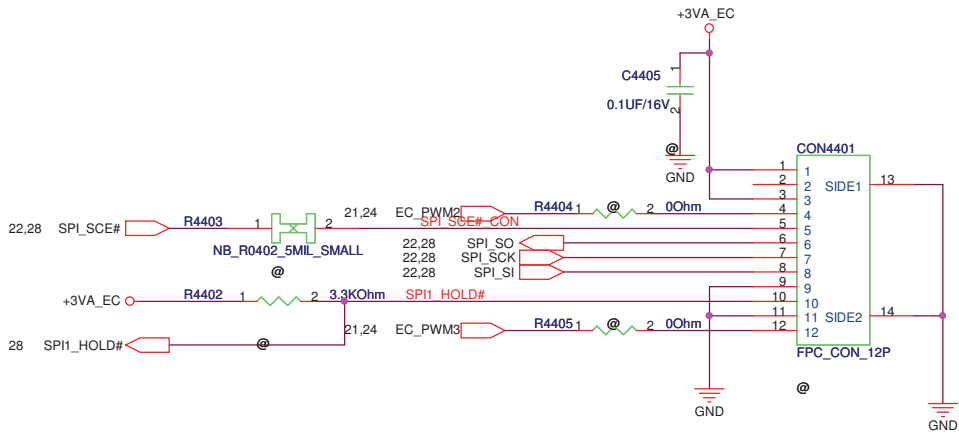
PEGATRON		Title : AUDIO CODEC-CX20671	
BG1		Engineer: <i>Alfie_Wang</i>	
Size	Project Name	Rev	
Custom	EABOO	2.0	
Date: Tuesday, January 25, 2011		Sheet	39 of 99



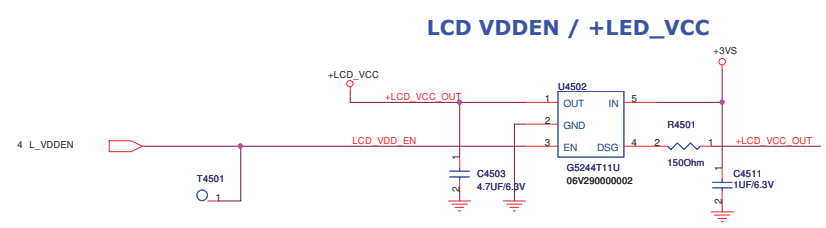
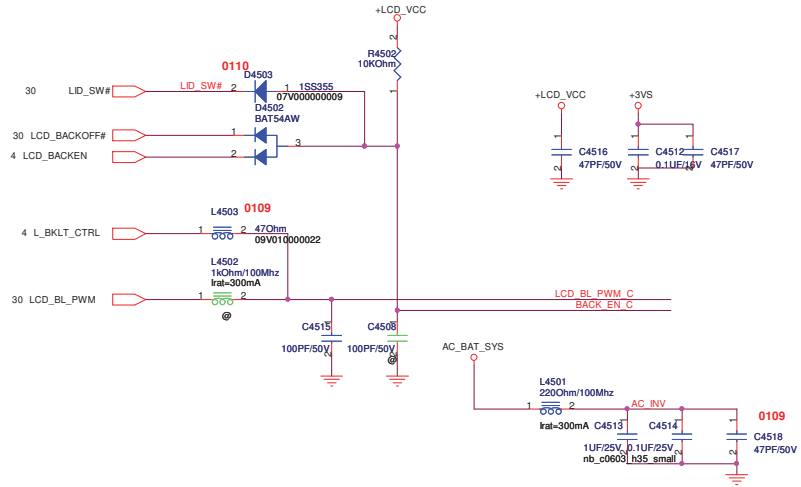
SP4	SD_D0
SP3	SD_D1
SP13	SD_D2
SP12	SD_D3
SP8	SD_CLK
SP1	SD_WP#
SP10	SD_CMD
SP6	SD_CD#



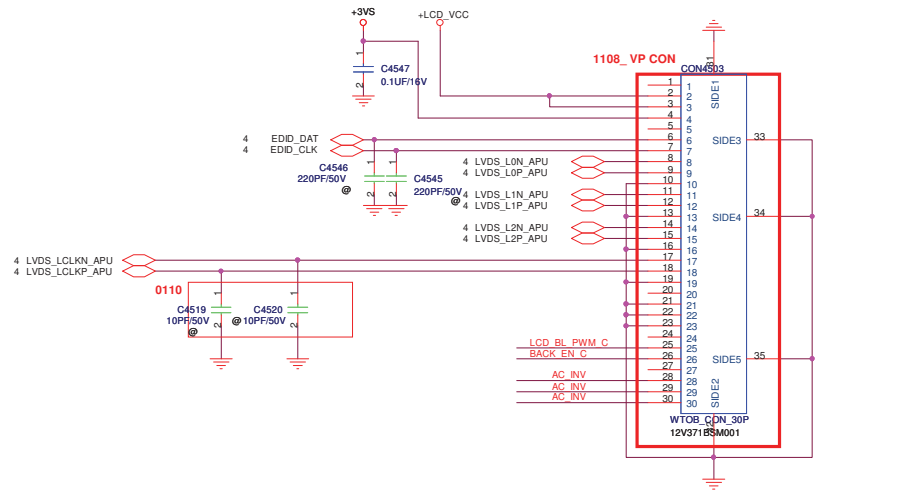
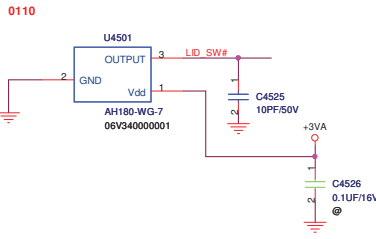
PEGATRON Title : RTS 5138		
PEGATRON CORPORATION		Engineer:
Size B	Project Name DESIGN IP	Rev 2.0
Date: Tuesday, January 25, 2011	Sheet 40	of 1



PEGATRON Title : DEBUG		
BG1		Engineer: Alfie Wang
Size B	Project Name EABOO	Rev 2.0
Date: Tuesday, January 25, 2011		Sheet 44 of 99



Hall Sensor



PEGATRON		Title : LVDS OUT	
BGI		Engineer: <i>Allie Wang</i>	
Size	Project Name	Rev	
Custom	EAB00	2.0	
Date: Tuesday, January 25, 2011		Sheet	45 of 99

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PEGATRON		Title : CRT	
BG1		Engineer: <i>Alfie Wang</i>	
Size	Project Name		Rev
Custom	EAB00		2.0
Date: Tuesday, January 25, 2011	Sheet	46	of 99

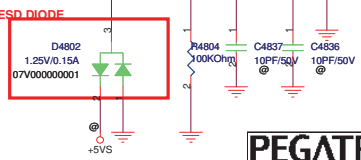
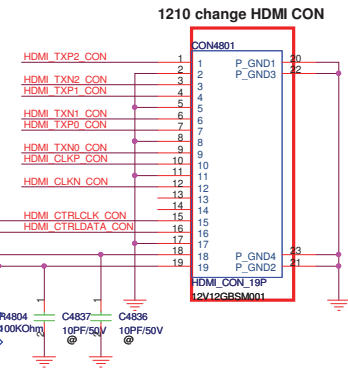
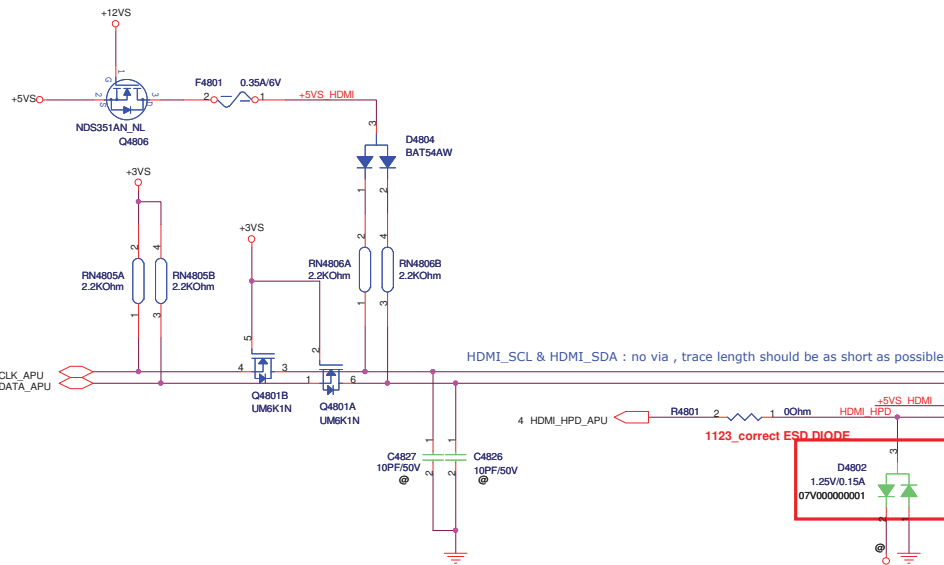
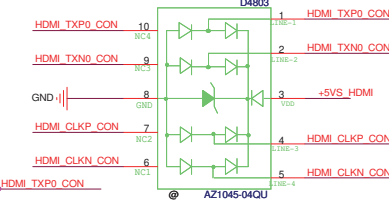
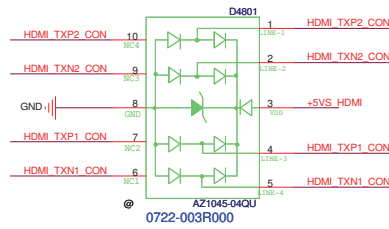
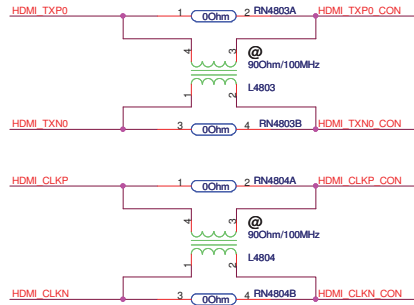
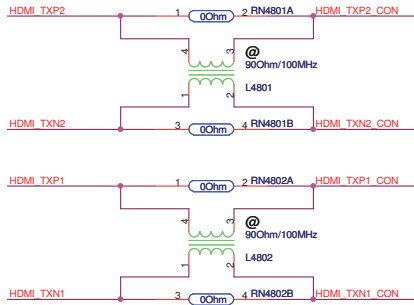
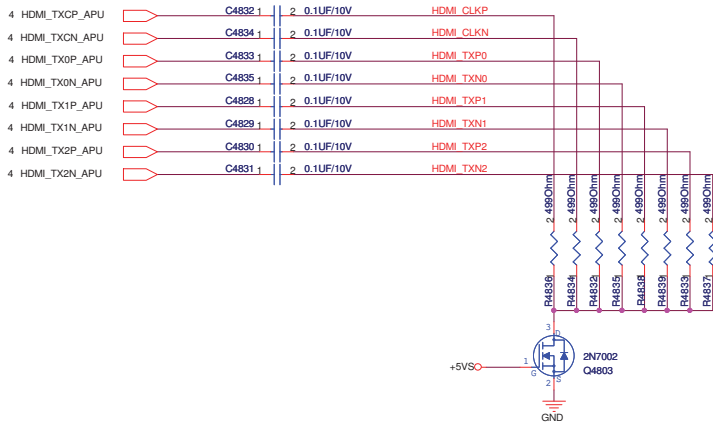
5

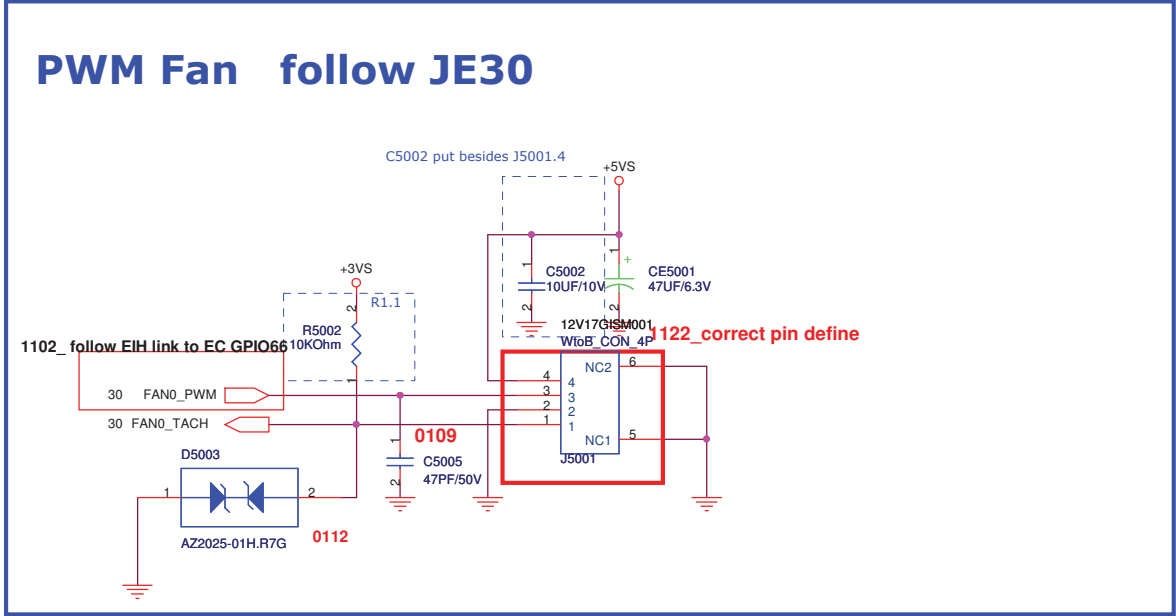
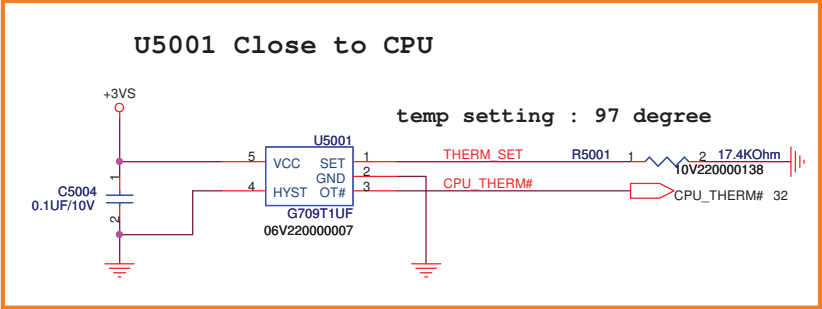
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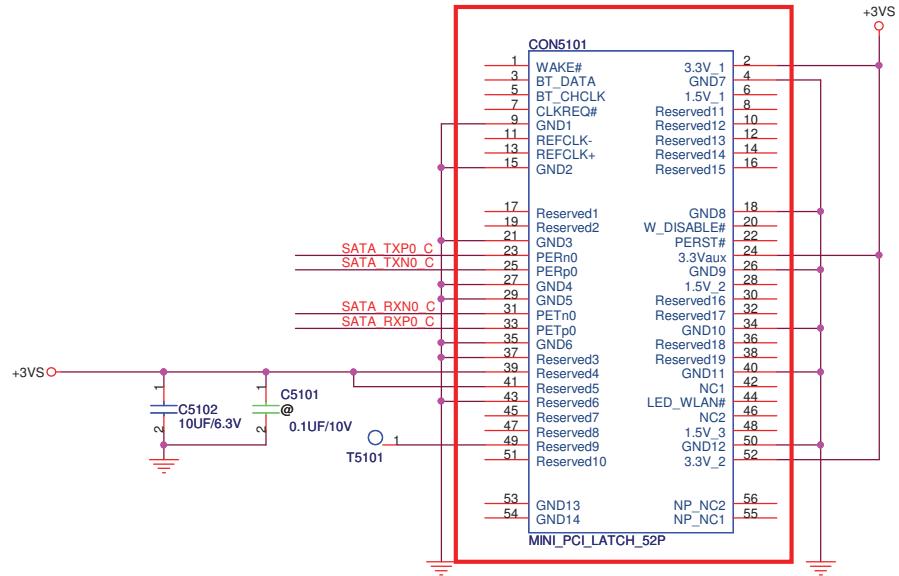
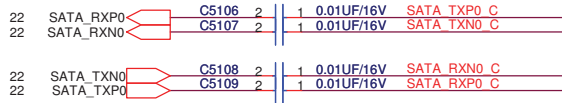




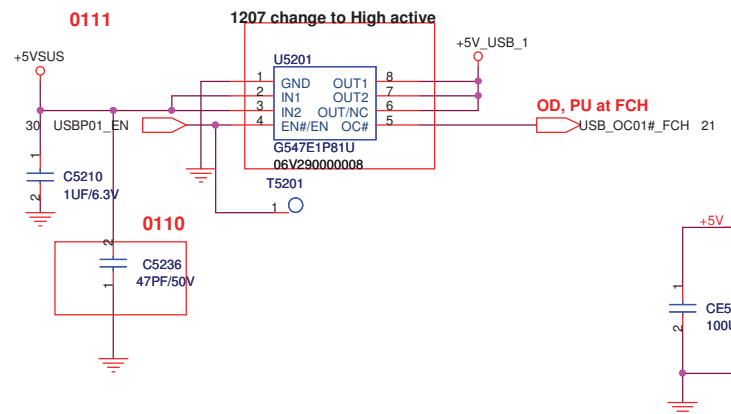
PEGATRON Title : FAN_Fan,Sensor		
Engineer: Alfie_Wang		
Size B	Project Name EAB00	Rev 2.0
Date: Tuesday, January 25, 2011 Sheet 50 of 99		

SSD

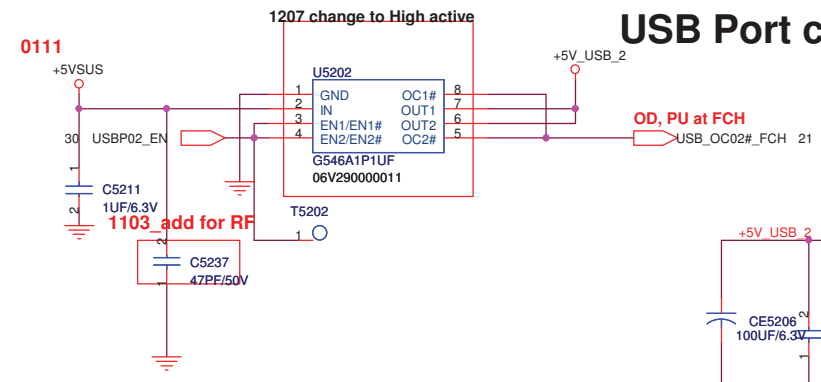
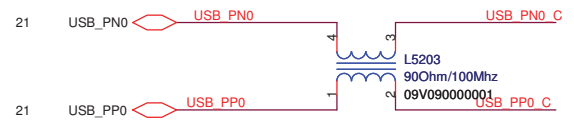
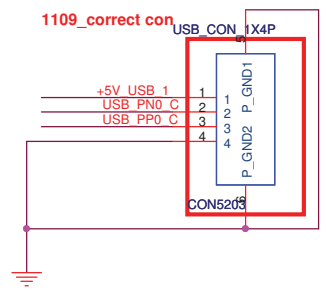
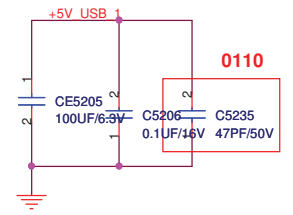
1106 pin define for SSD check OK, change ME correct CON.



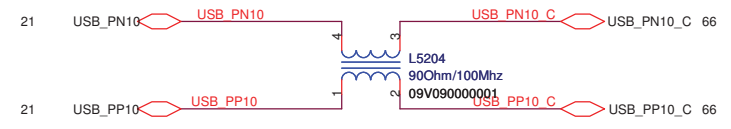
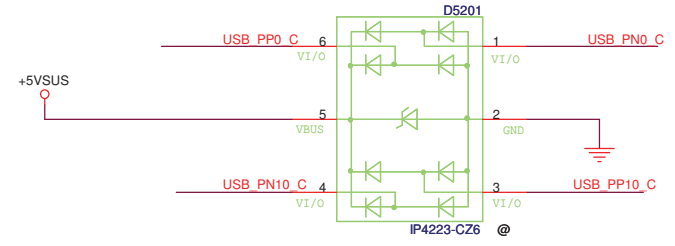
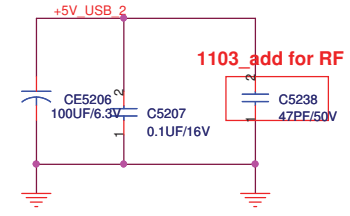
PEGATRON Title : SSD(mSATA)		
BG1		Engineer: Alfie Wang
Size B	Project Name EABOO	Rev 2.0
Date: Tuesday, January 25, 2011		Sheet 51 of 99



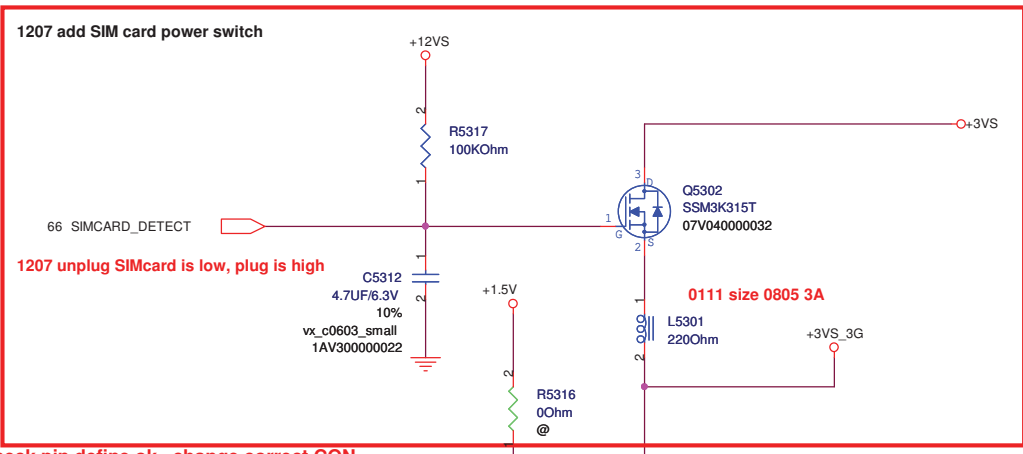
USB 2.0 (1213-00JP000)



USB Port current limit

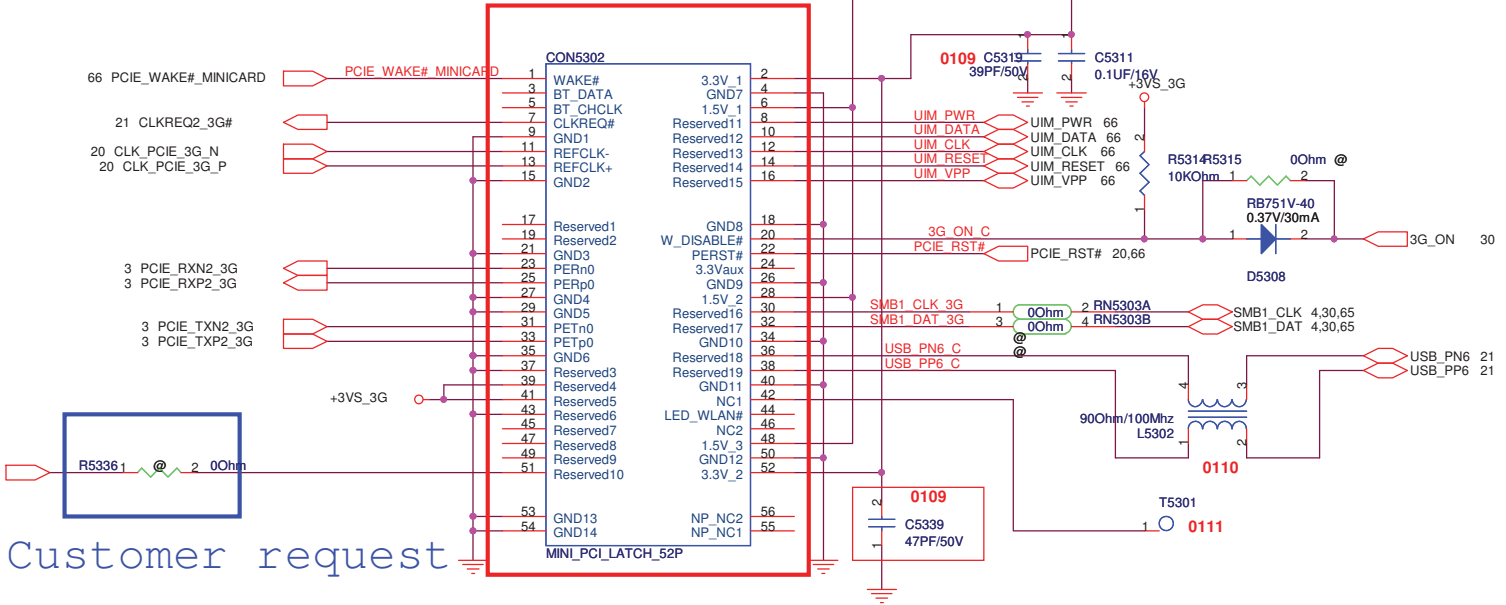


PEGATRON Title :USB JACK		Rev 2.0
BG1 Engineer: <i>Alfie_Wang</i>		
Size B	Project Name EAB00	
Date: Tuesday, January 25, 2011	Sheet 52 of 99	



3G

1029_check pin define ok , change correct CON

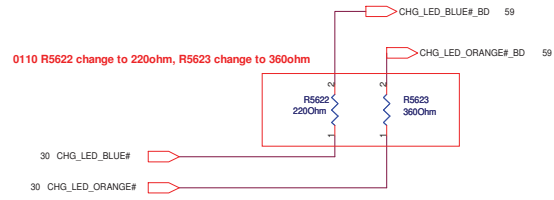


PEGATRON Title : 3G Full Minicard		
BG1		Engineer: <i>Alfie Wang</i>
Size	Project Name	Rev
B	EAB00	2.0
Date: Tuesday, January 25, 2011		Sheet 53 of 99



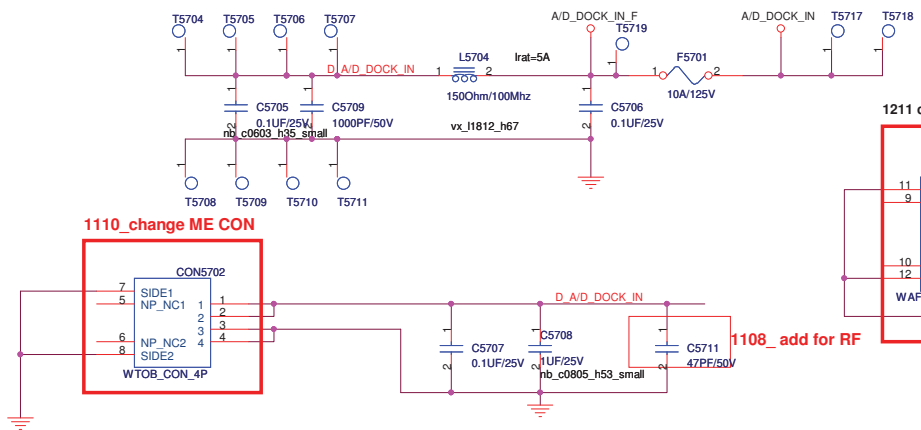
PEGATRON		Title : SSD to SATA	
BG1		Engineer: Alfie_Wang	
Size	Project Name	Rev	
Custom	EAB00	2.0	
Date: Tuesday, January 25, 2011		Sheet	54 of 99

Charger LED

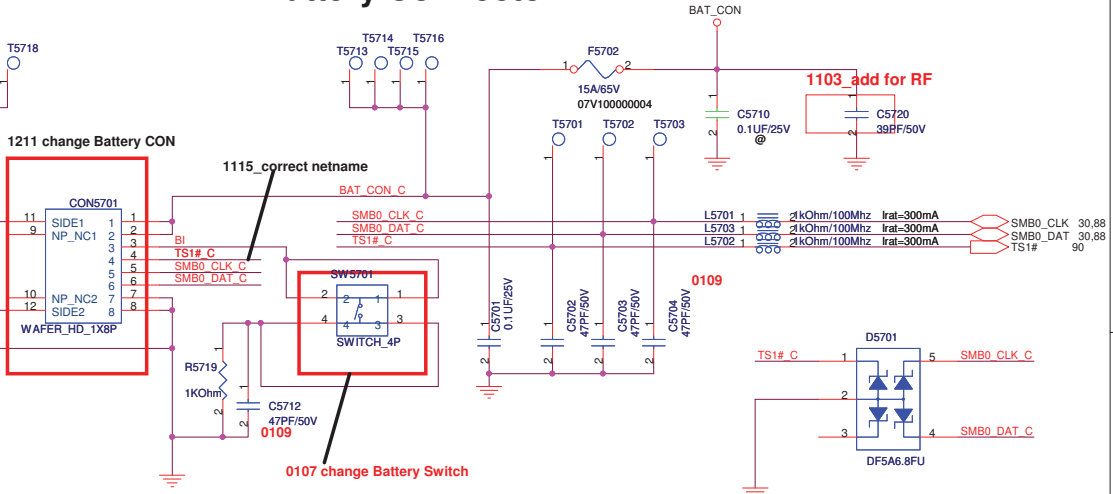


Dual Color

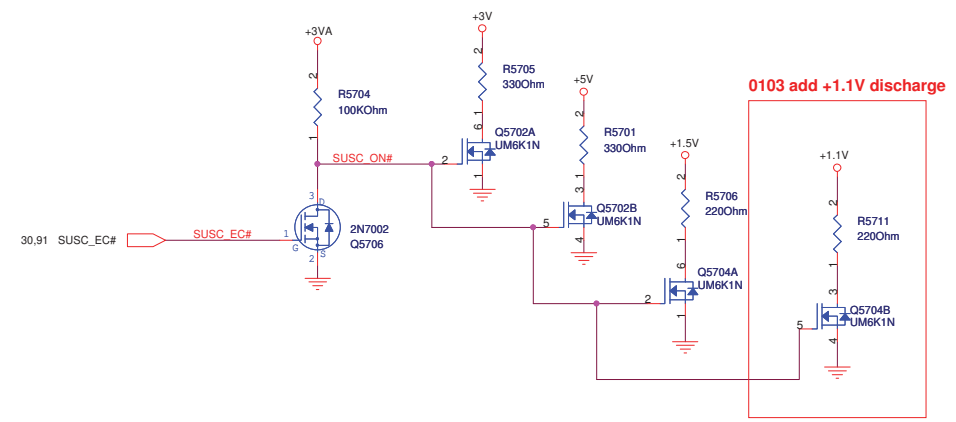
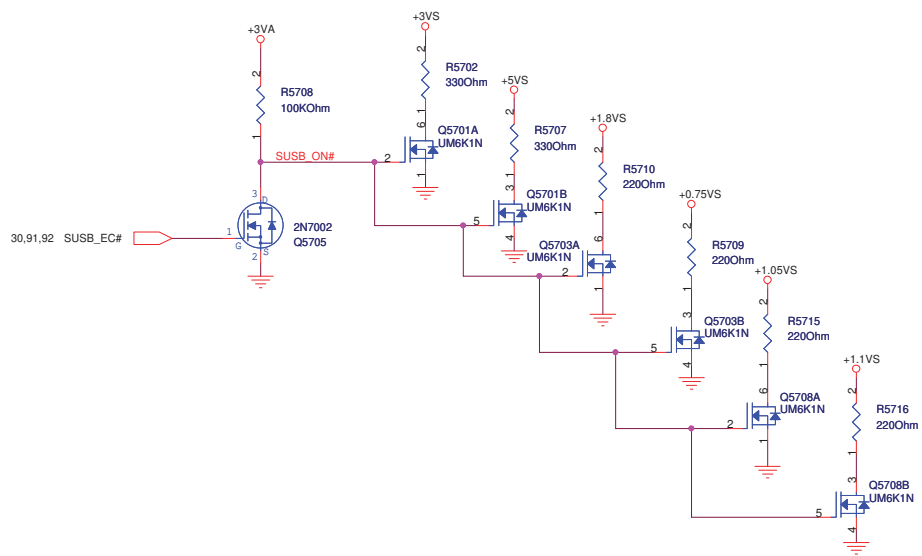
DC IN



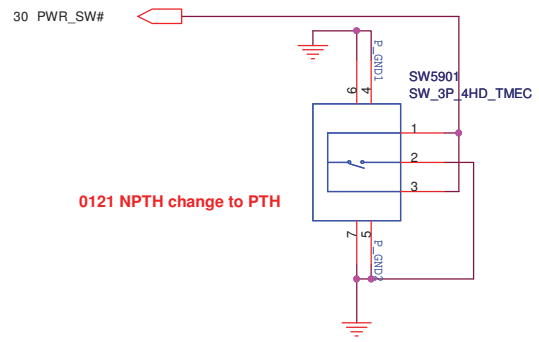
Battery Connector



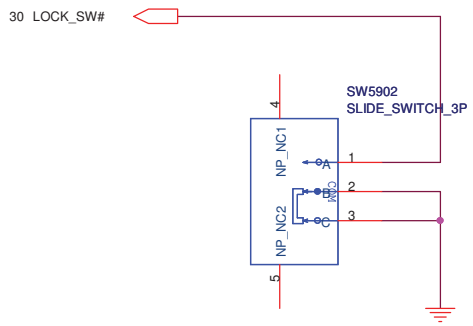
Discharge Circuit



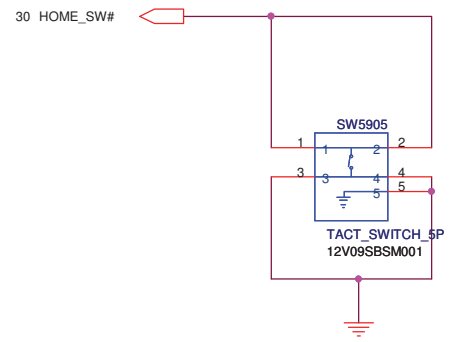
POWER SW



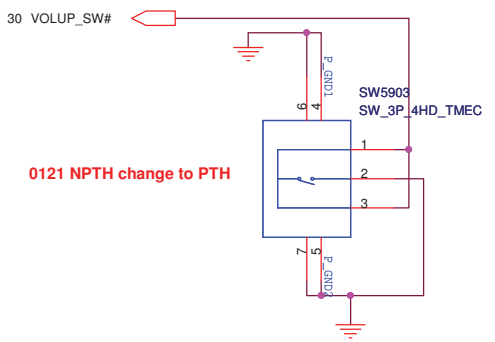
LOCK SLIDE SWITCH



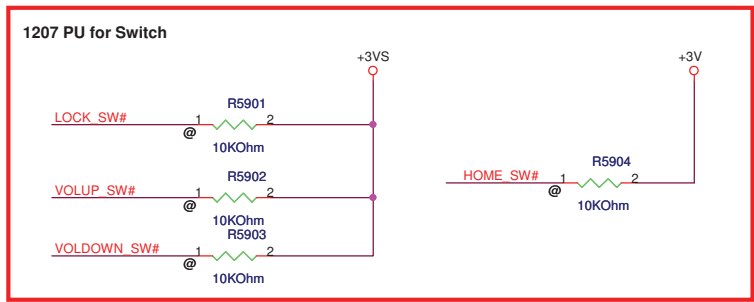
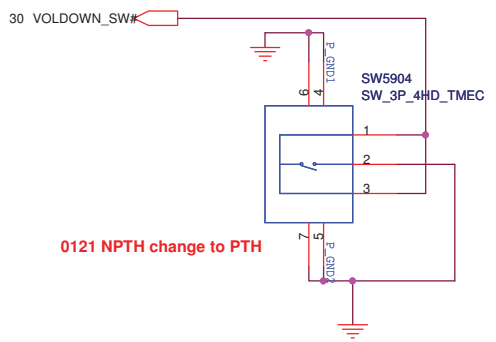
HOME BTN



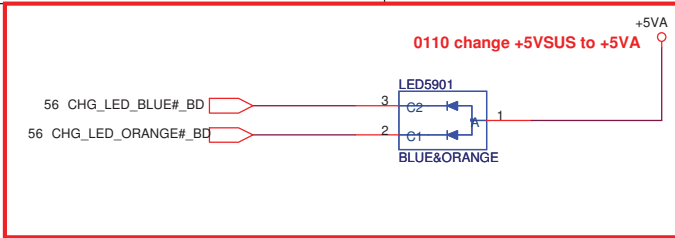
Volume UP



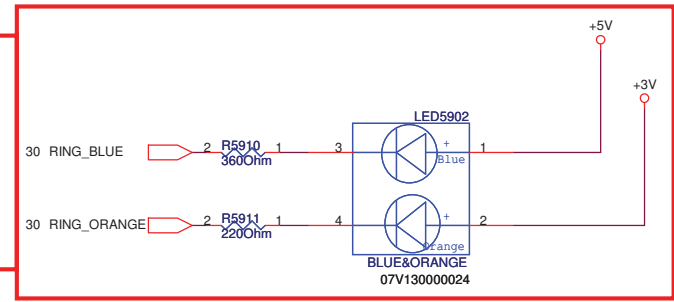
Volume DOWN



1213 Power SW LED



1213 HOME SW LED



PEGATRON Title :SW & BTN	
BG1	Engineer: <i>Alfie_Wang</i>
Size B	Project Name EAB00
Date: Tuesday, January 25, 2011	Rev 2.0
Sheet 59	of 99

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PEGATRON Title : SAR		
BG1		Engineer: <i>Alfie_Wang</i>
Size B	Project Name EABOO	Rev 2.0
Date: <i>Tuesday, January 25, 2011</i>		Sheet 60 of 99

5

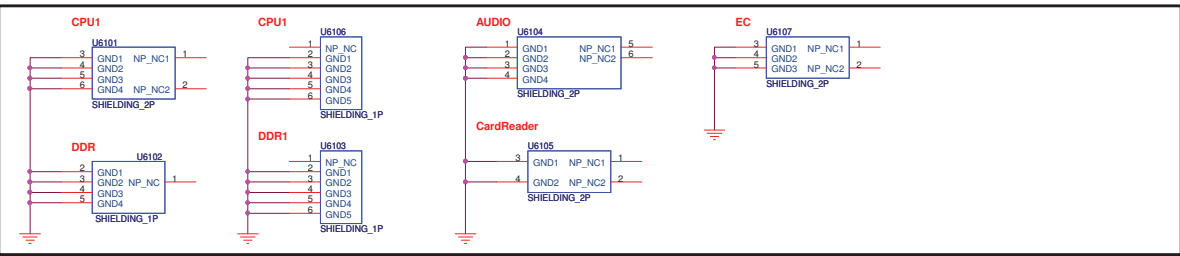
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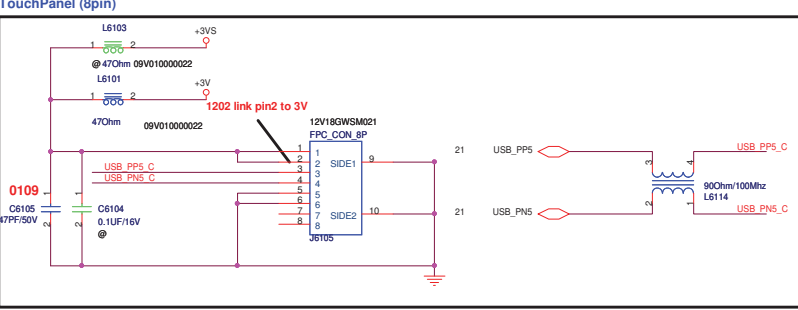
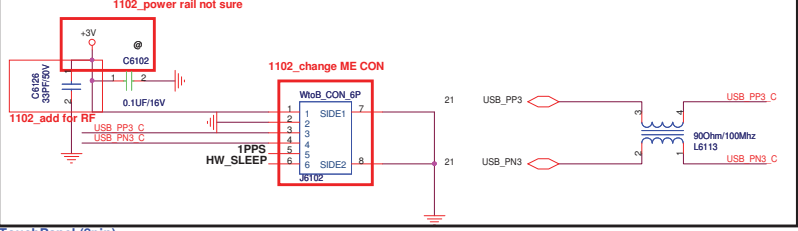
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Shielding Case



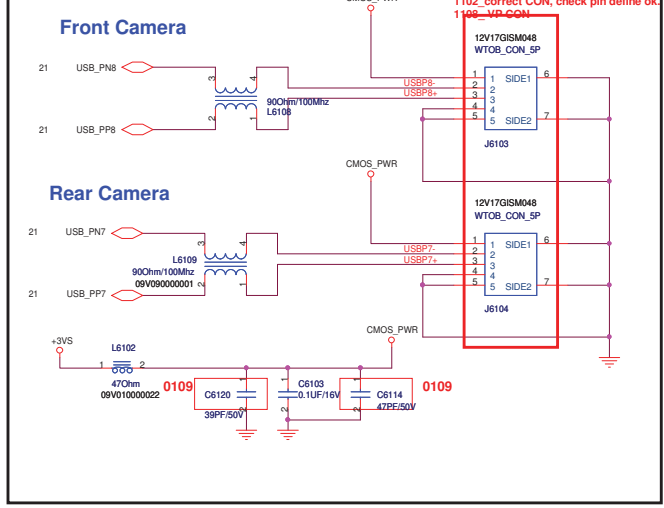
GPS



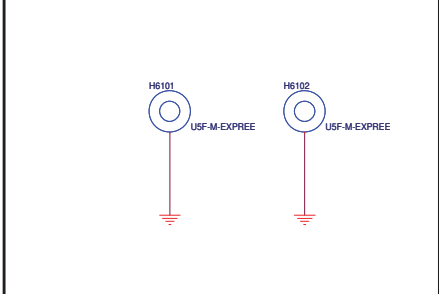
LED Board (12pin)
 1230 remove CON6105

BT CON
 1210 remove BT

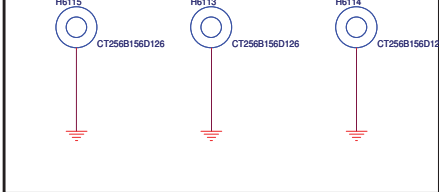
CMOS



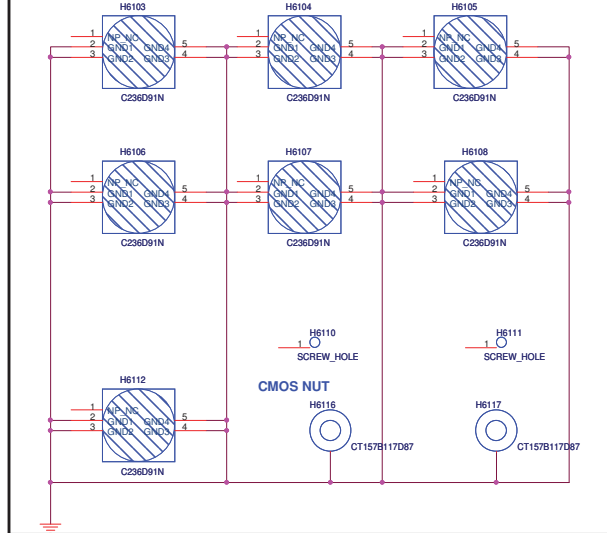
SSD,3G NUT



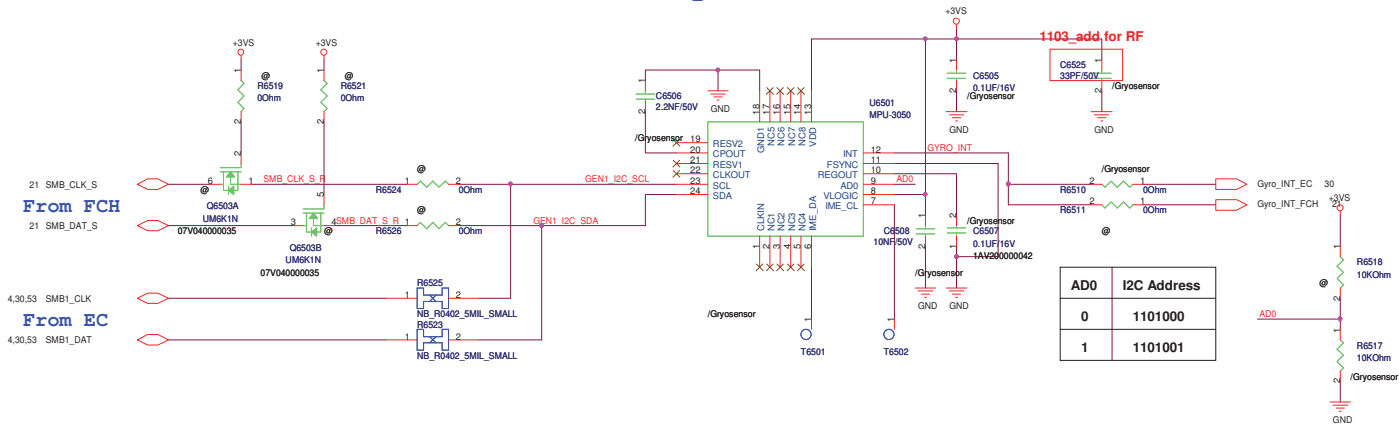
CPU NUT



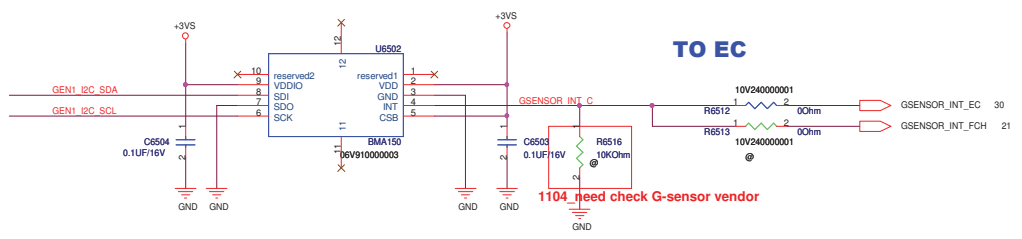
Screw hole



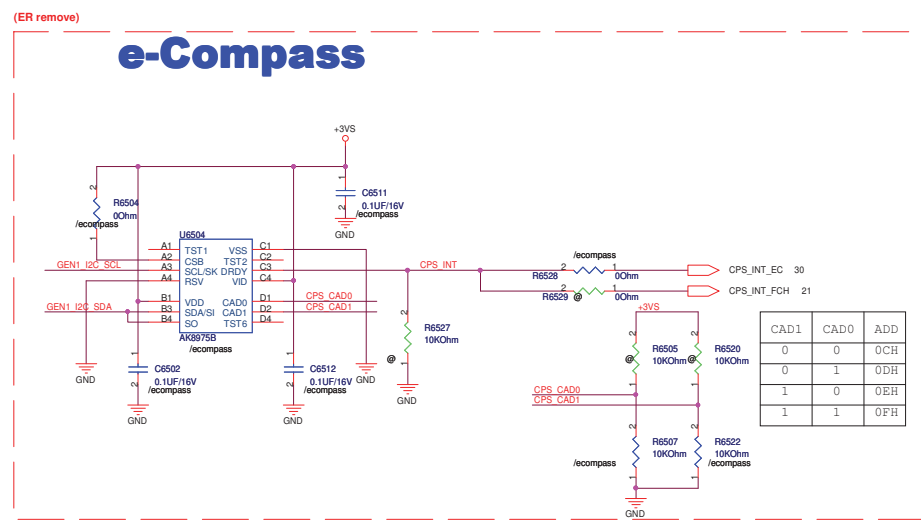
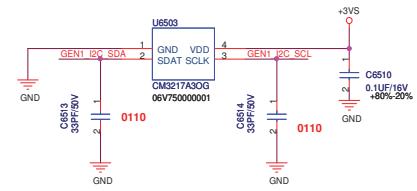
(ER remove) **Gyro-sensor**



G-sensor

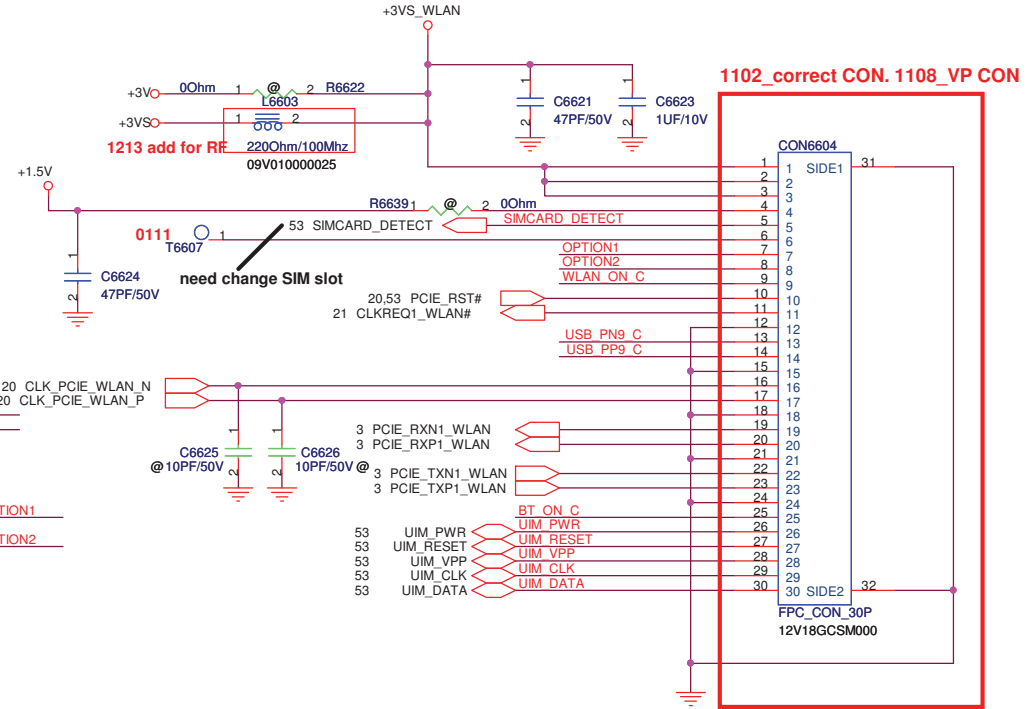
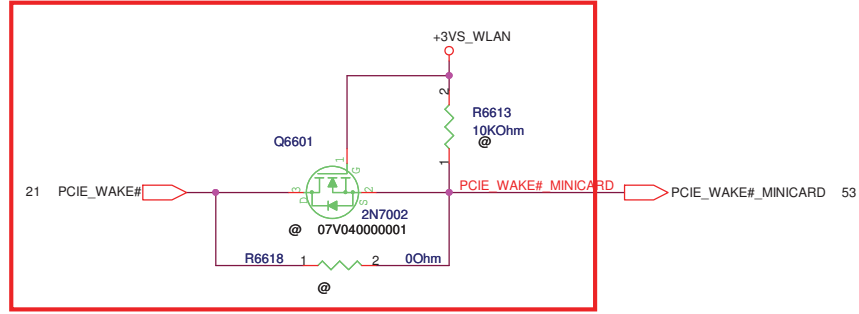


Light-sensor



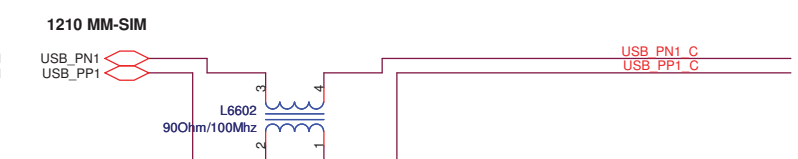
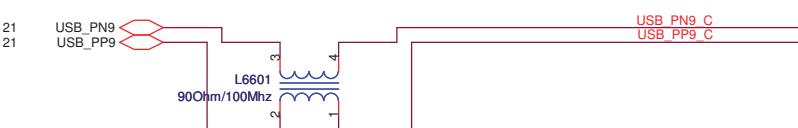
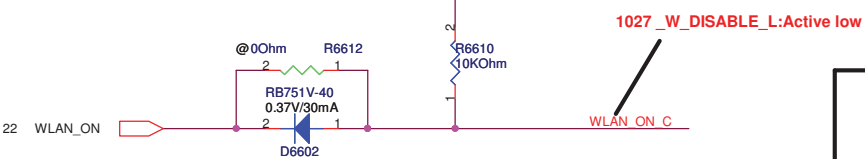
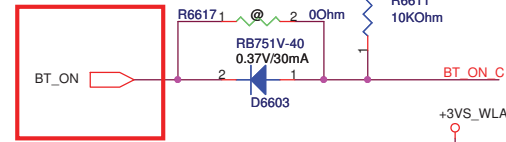
Minicard CON 30pins

1027_WB214E pin1 is NC

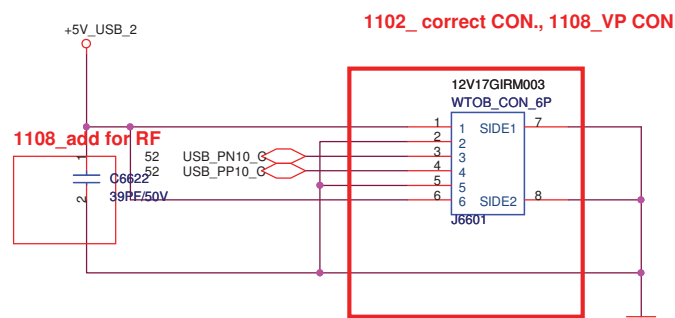


Customer request

1027_change to BT_ON# for WB214E

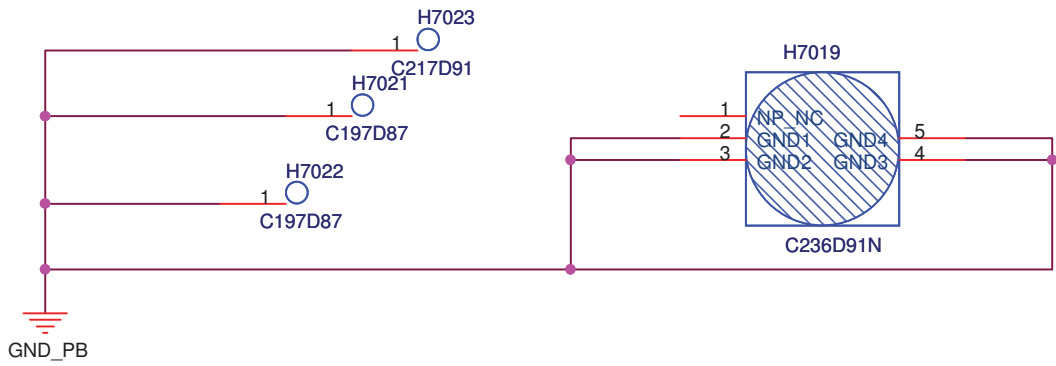
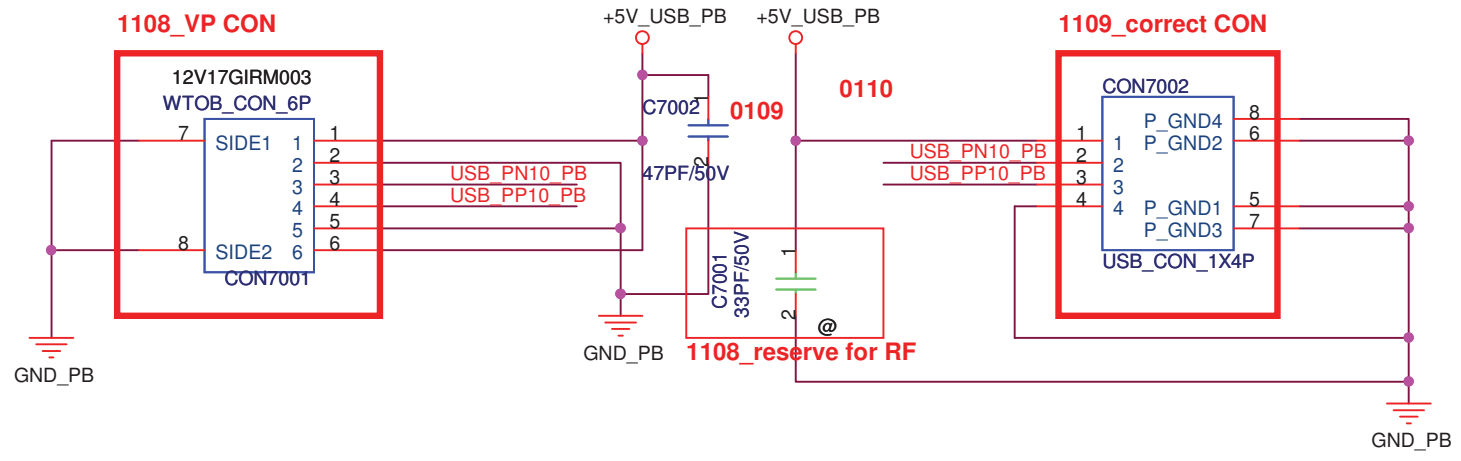


USB Port CON 6pins

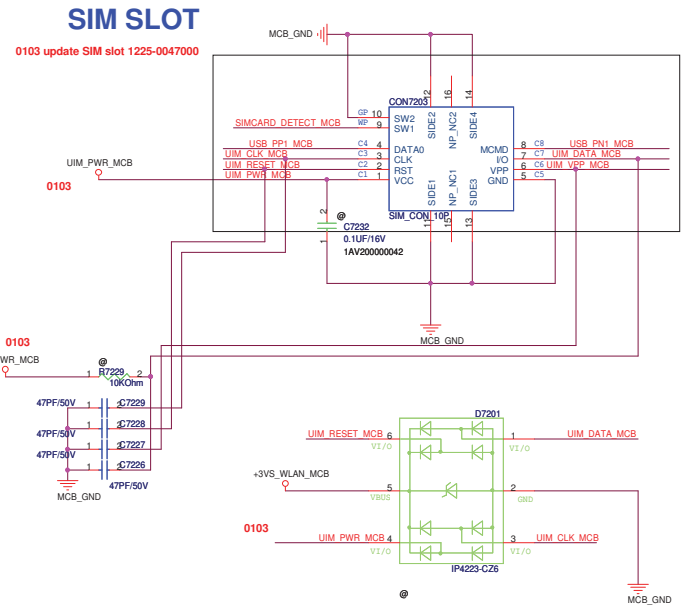
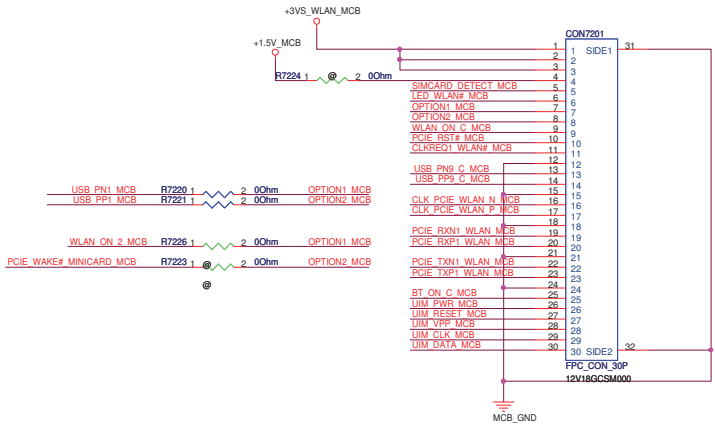


PEGATRON Title :WTB CON	
BG1 Engineer: Alfie_Wang	
Size B	Project Name EAB00
Date: Tuesday, January 25, 2011	Rev 2.0
Sheet 66 of 99	

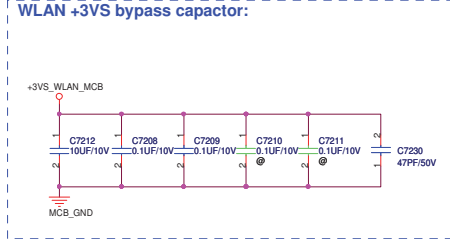
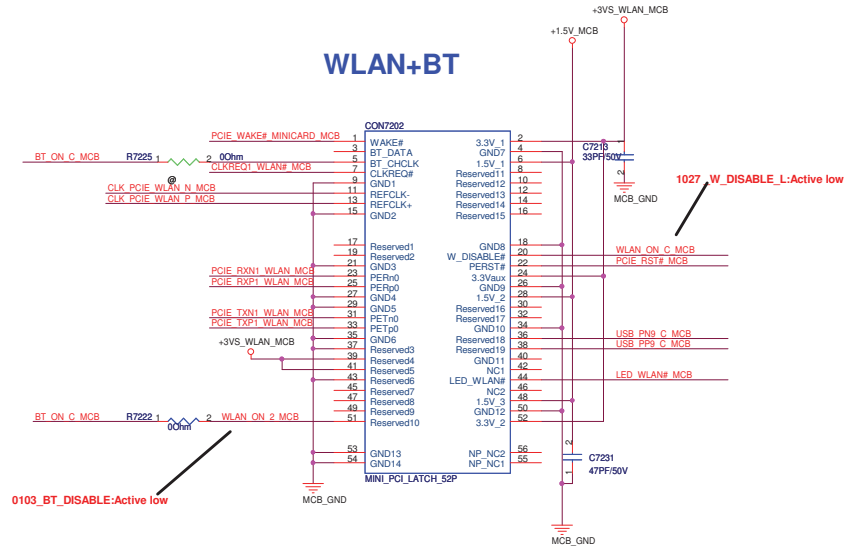
USB 2.0 for Docking Port



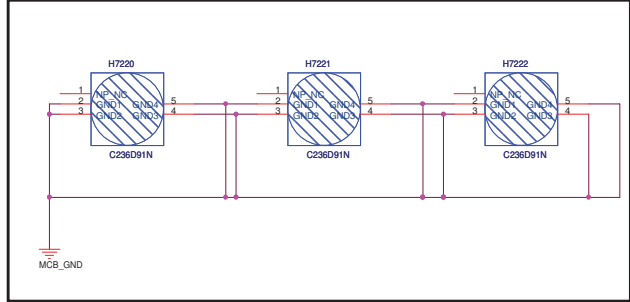
PEGATRON		Title : USB Docking Port	
BG1		Engineer: <i>Alfie_Wang</i>	
Size A	Project Name EABOO		Rev 2.0
Date: Tuesday, January 25, 2011		Sheet	70 of 99

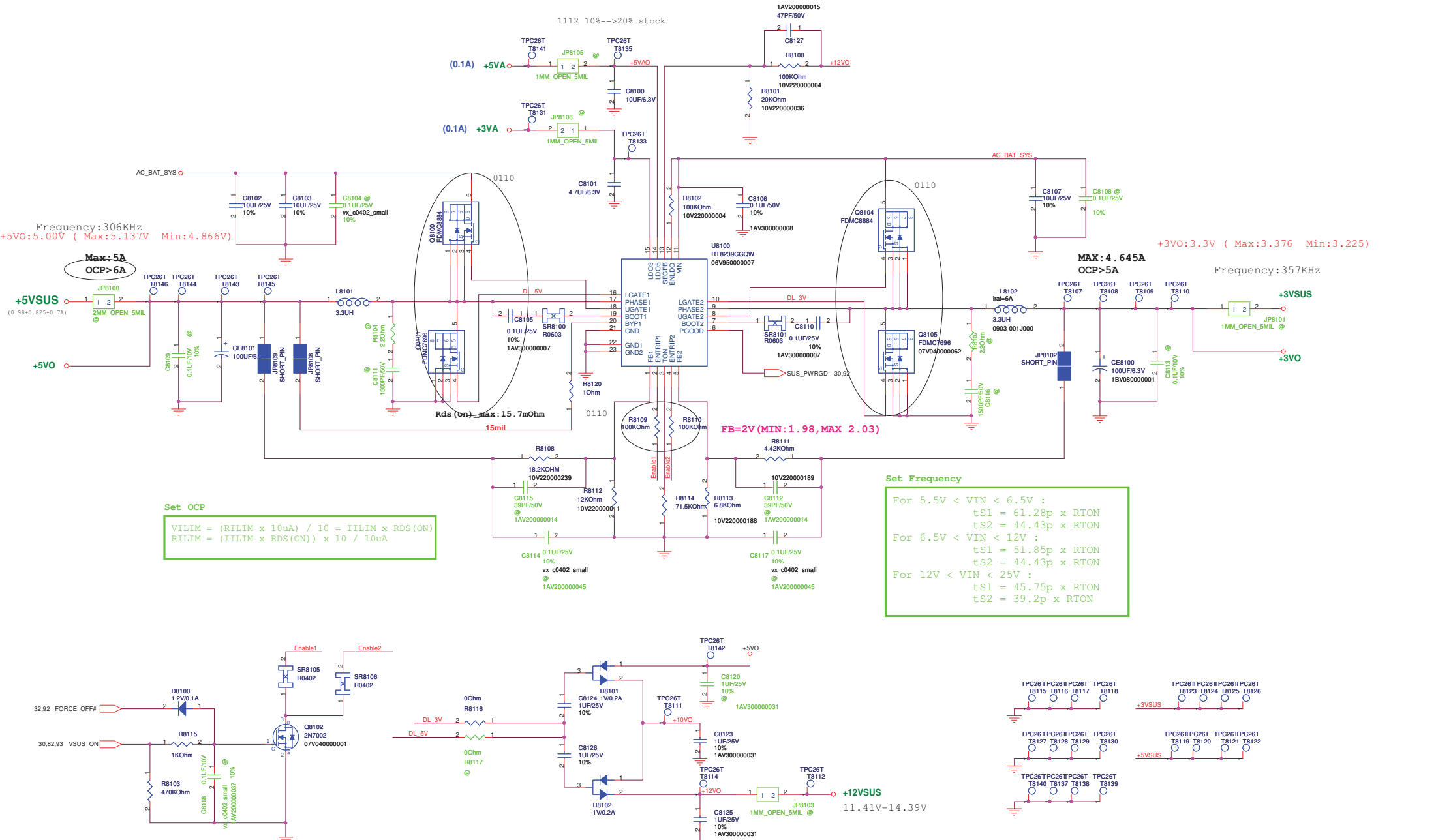


WLAN+BT



Screw hole





Frequency: 306KHz
 +5V0: 5.00V (Max: 5.137V Min: 4.866V)

Max: 5A
 OCP > 6A

+3V0: 3.3V (Max: 3.376 Min: 3.225)

MAX: 4.645A
 OCP > 5A

Frequency: 357KHz

Set OCP

$$VILIM = (RILIM \times 10\mu A) / 10 = IILIM \times RDS(ON)$$

$$RILIM = (IILIM \times RDS(ON)) \times 10 / 10\mu A$$

Set Frequency

For $5.5V < VIN < 6.5V$:

$$ts1 = 61.28p \times RTON$$

$$ts2 = 44.43p \times RTON$$

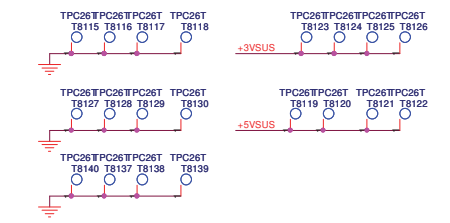
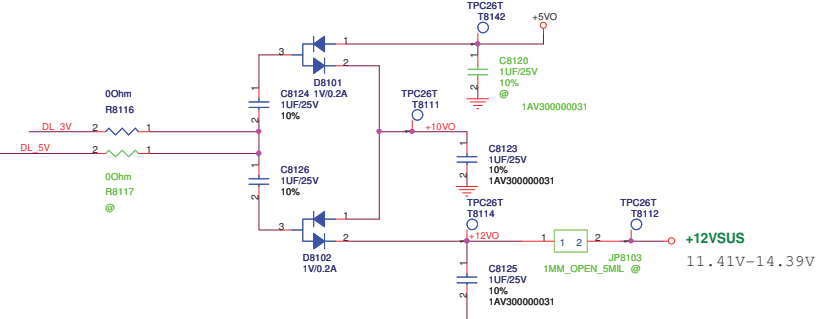
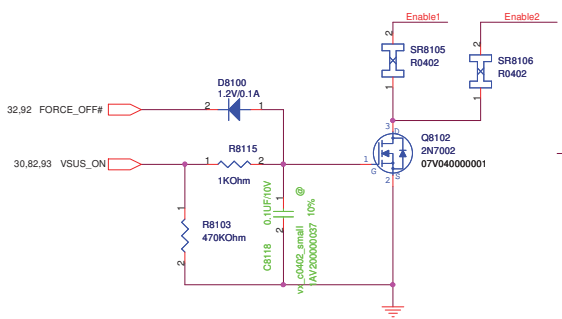
For $6.5V < VIN < 12V$:

$$ts1 = 51.85p \times RTON$$

$$ts2 = 44.43p \times RTON$$

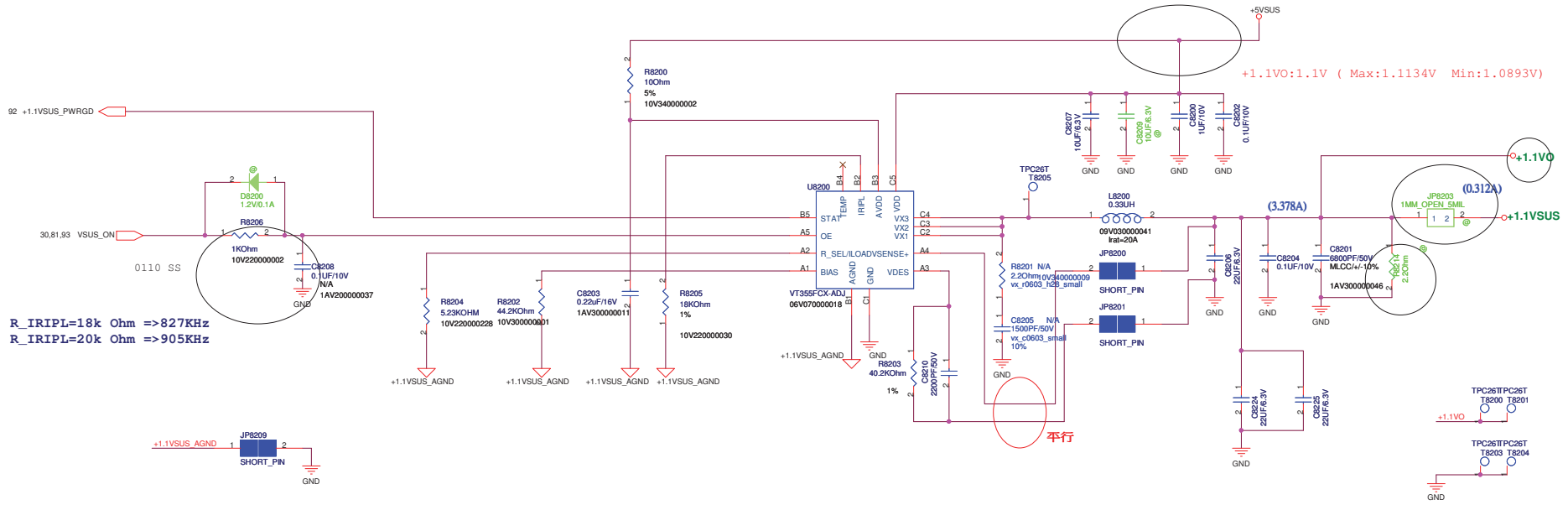
For $12V < VIN < 25V$:

$$ts1 = 45.75p \times RTON$$

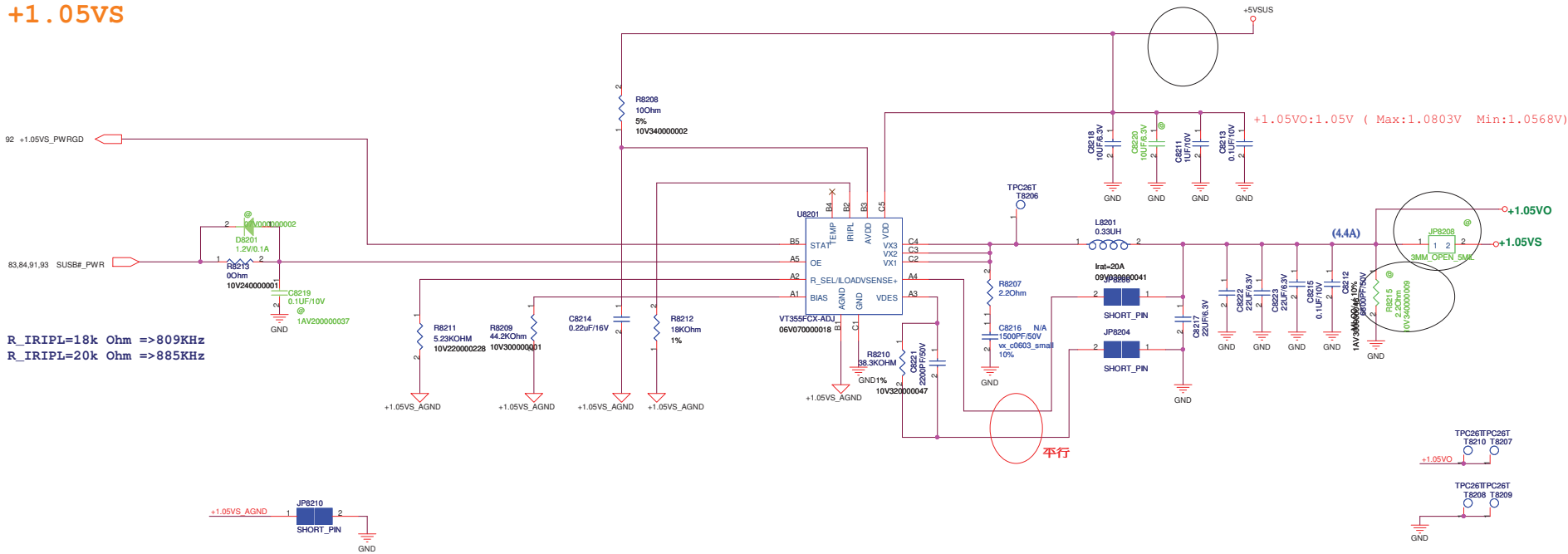
$$ts2 = 39.2p \times RTON$$


+1.1VSUS

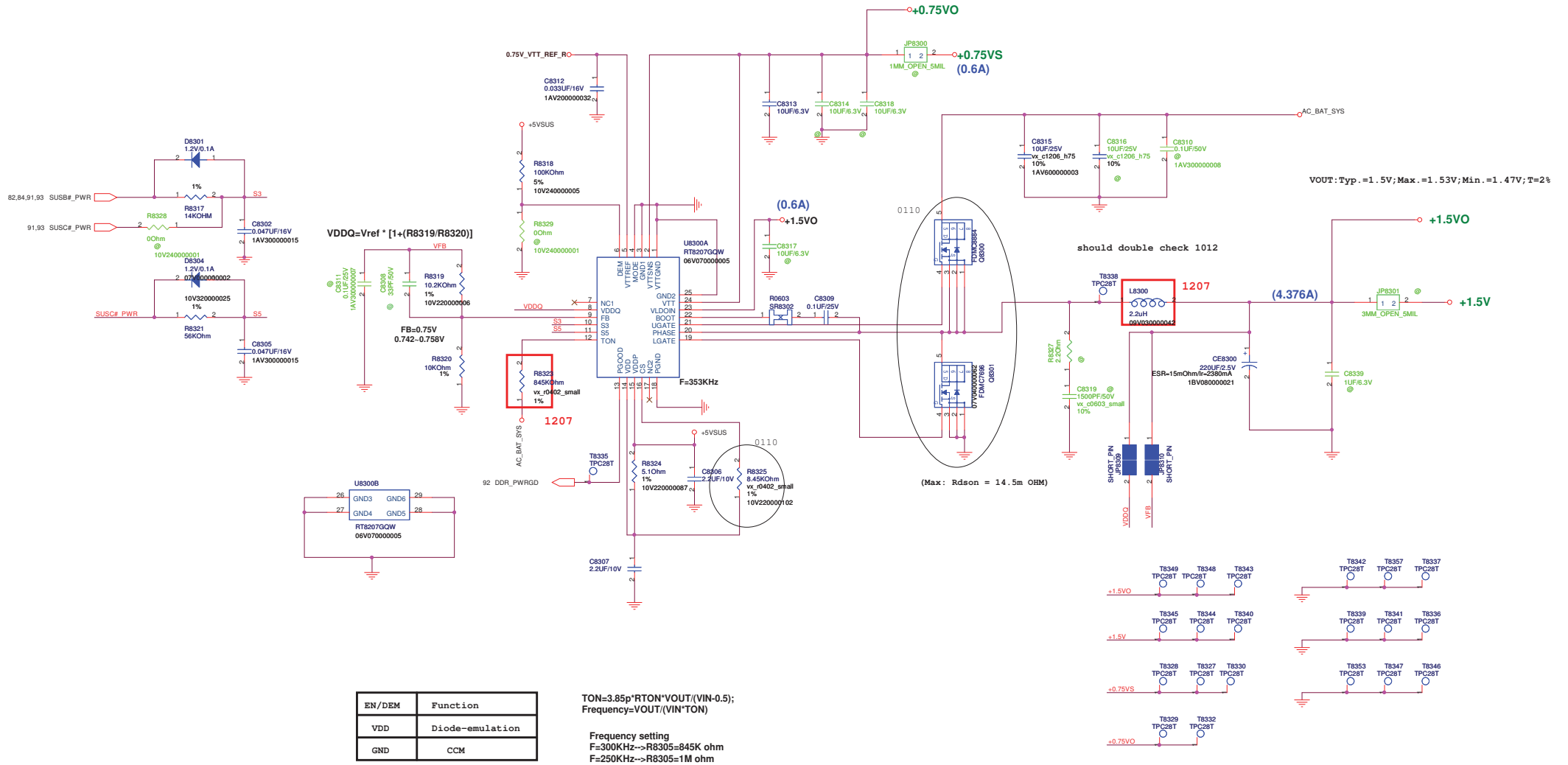
+1.1V & +1.05VS POWER SUPPLY



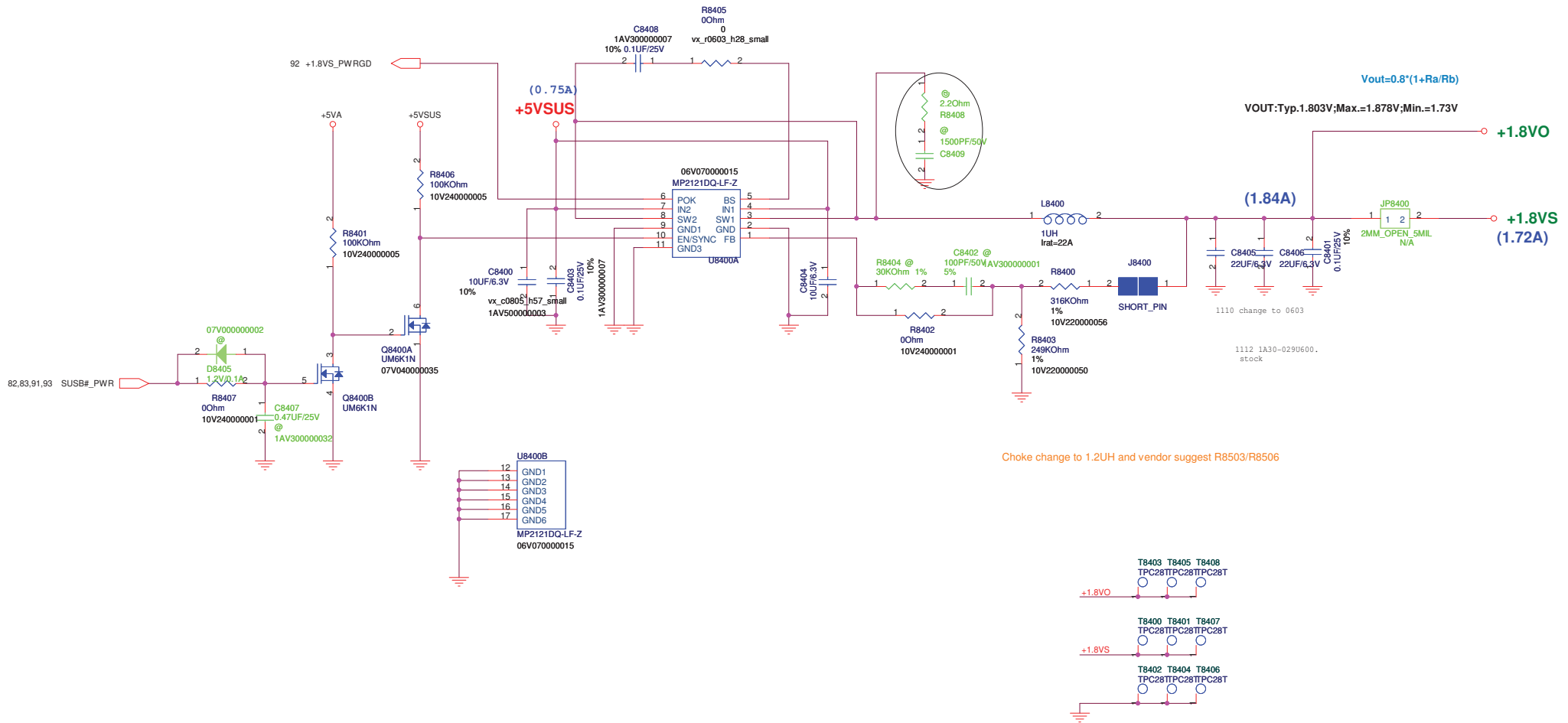
+1.05VS

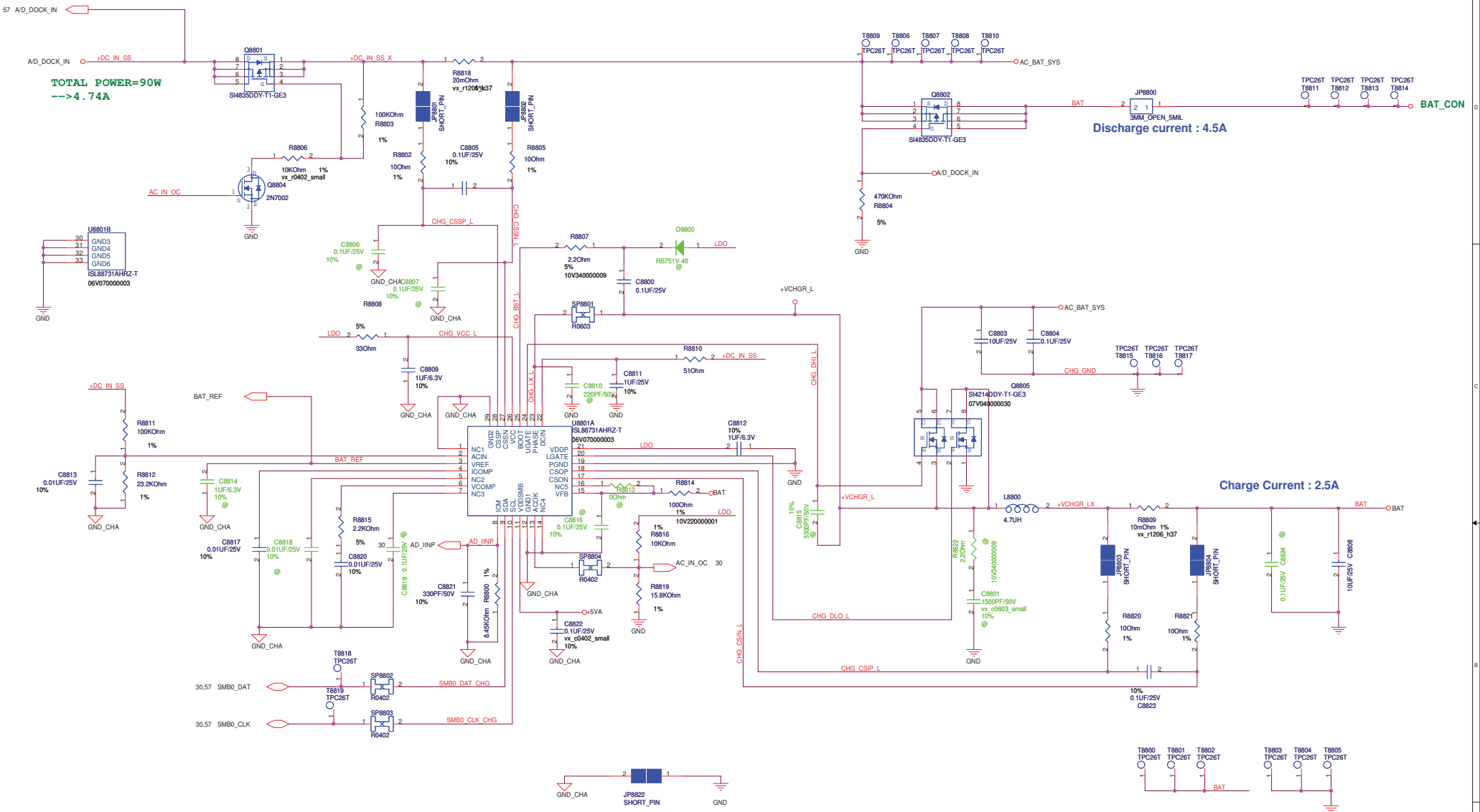


+1.5VO & +0.75VS POWER SUPPLY



+1.8VS POWER SUPPLY





TOTAL POWER=90W
 --> 4.74A

Discharge current : 4.5A

Charge Current : 2.5A

~Variant Name~

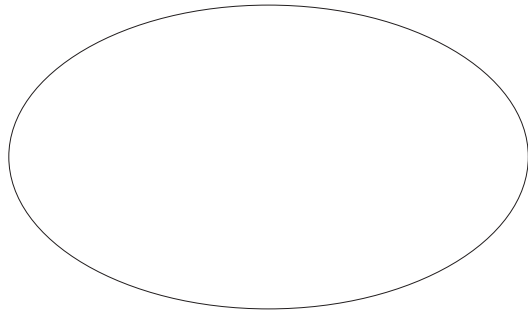
PEGATRON Title : POWER CHARGER		
Engineer: Louis		
Size C	Project Name EAB00	Rev 1.0
Date: Tuesday, January 25, 2011	Sheet	88 of 99

BATTERY IN DETECT

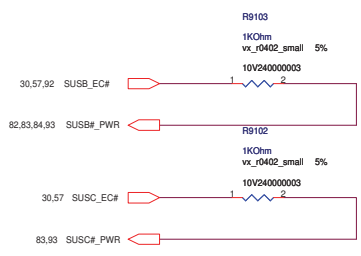
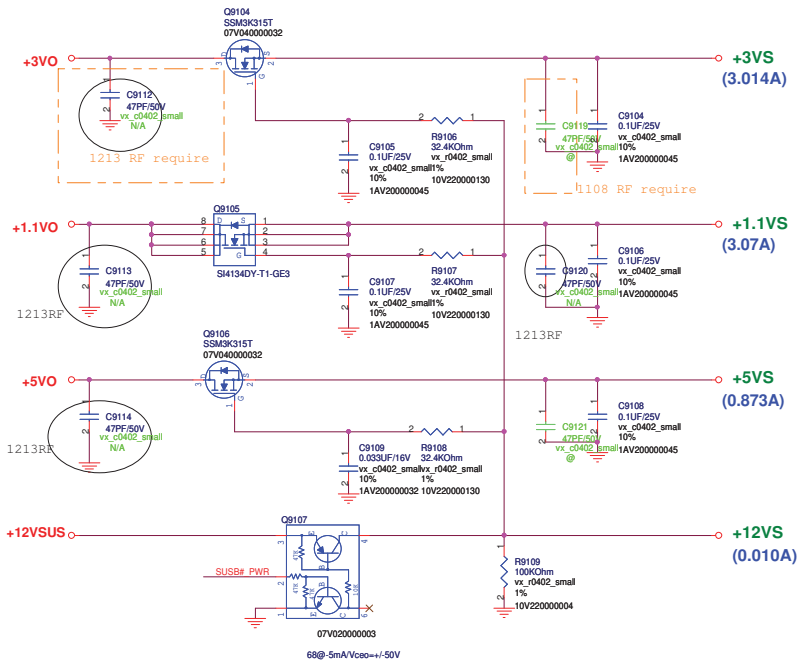


POWER LIMIT CIRCUIT

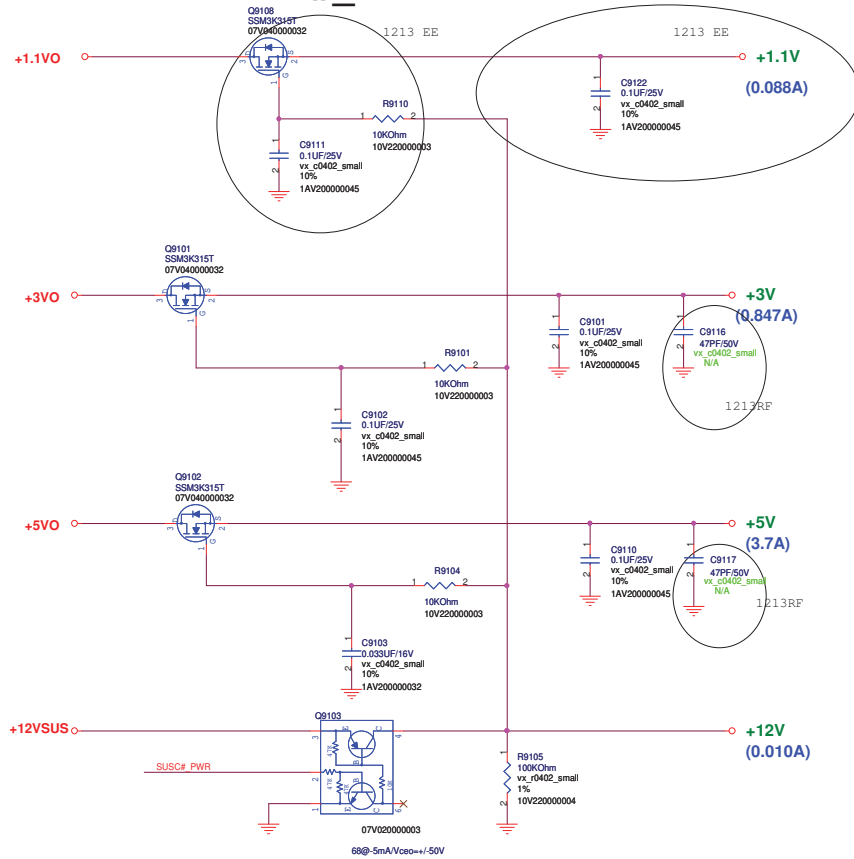
+2.5Vref delete



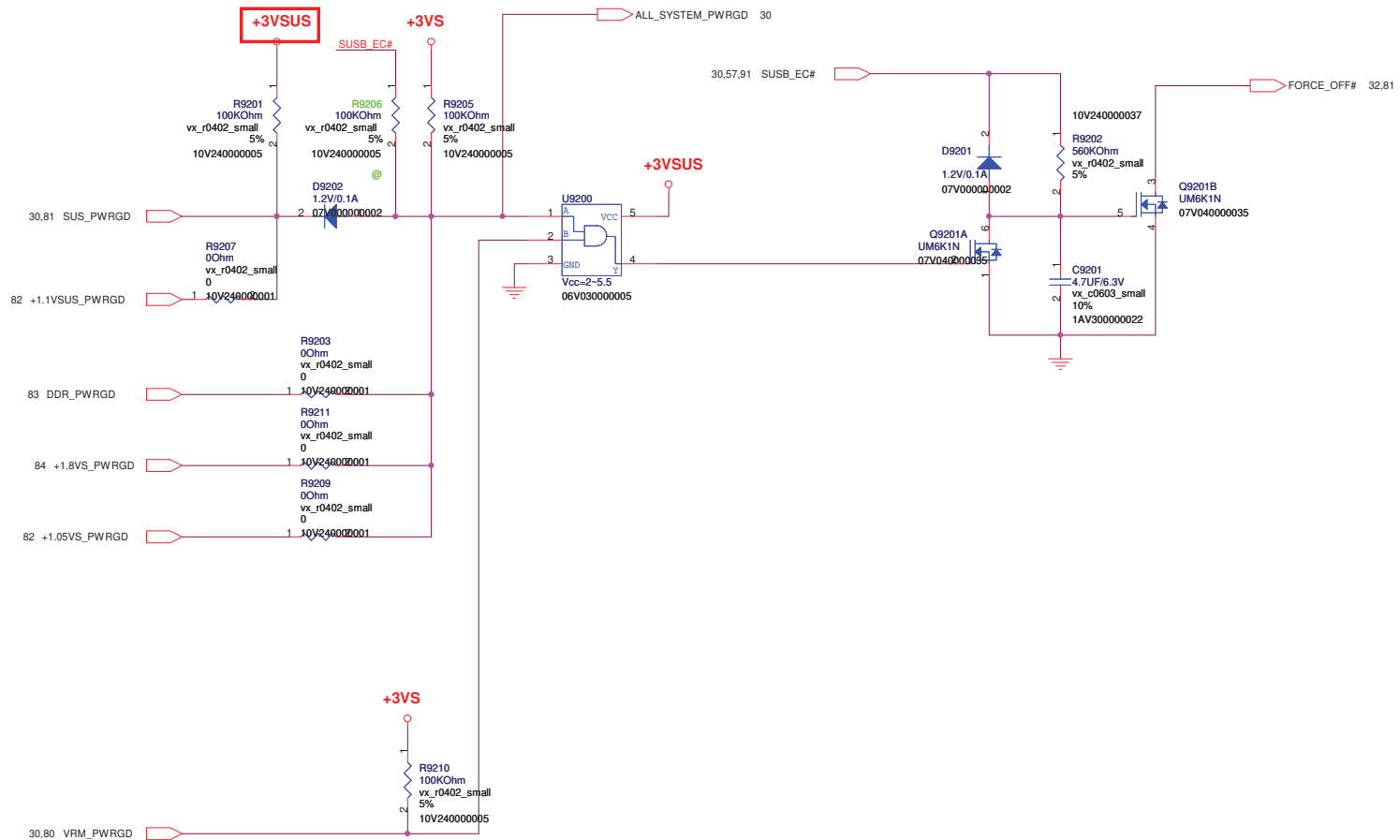
SUSB#_PWR POWER

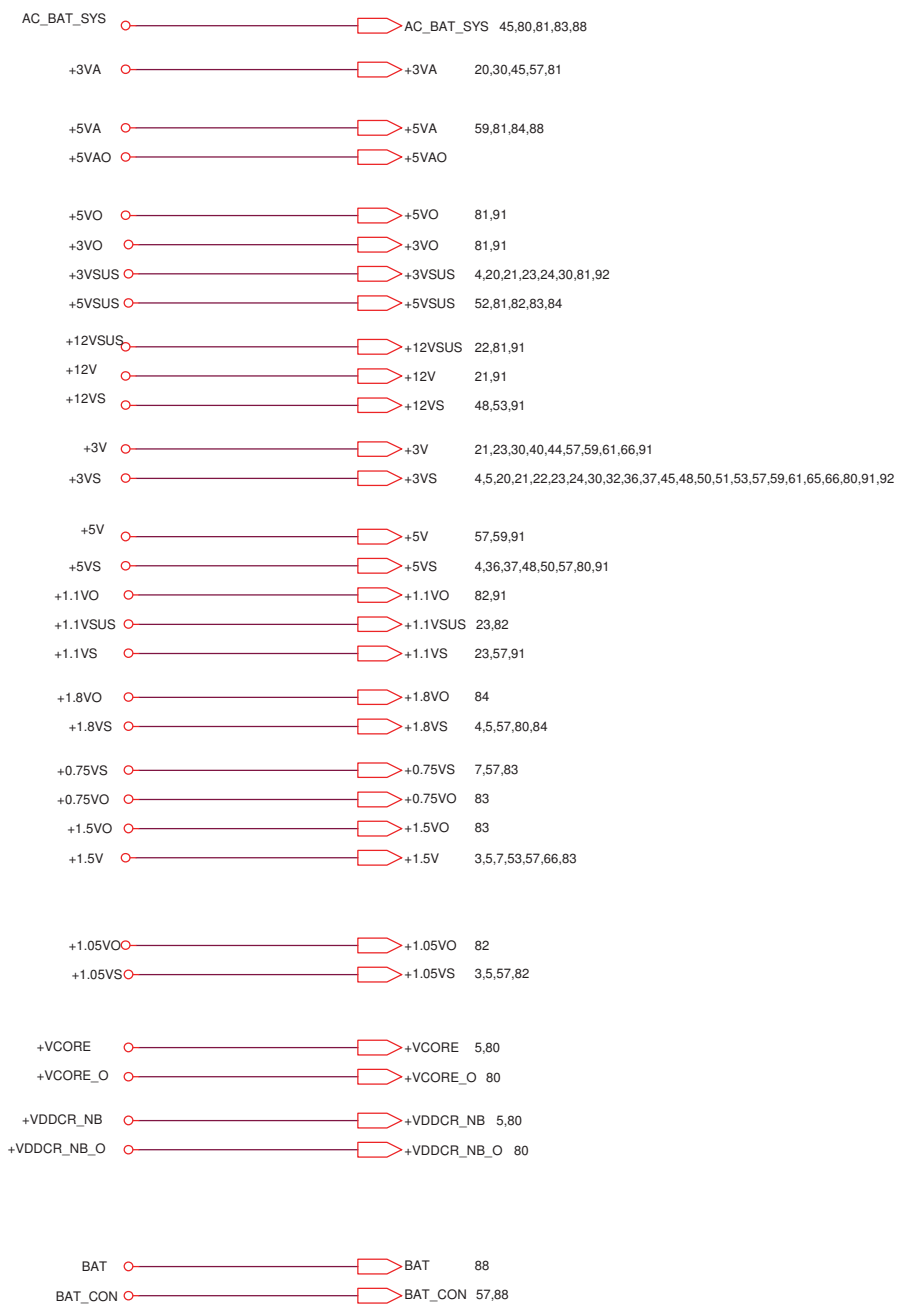


SUSC#_PWR POWER

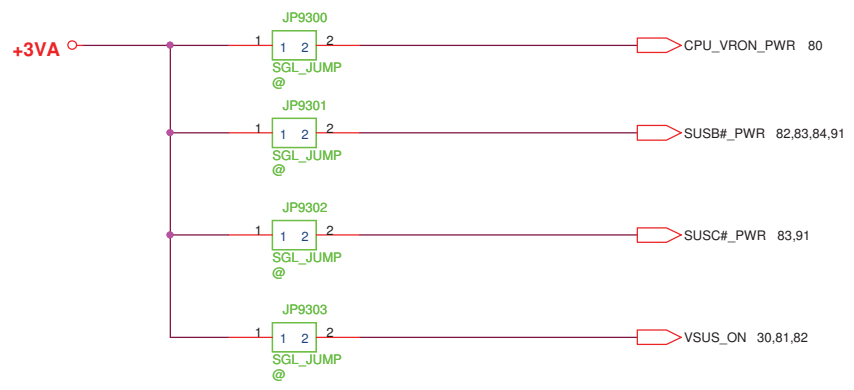


POWER GOOD DETECTOR



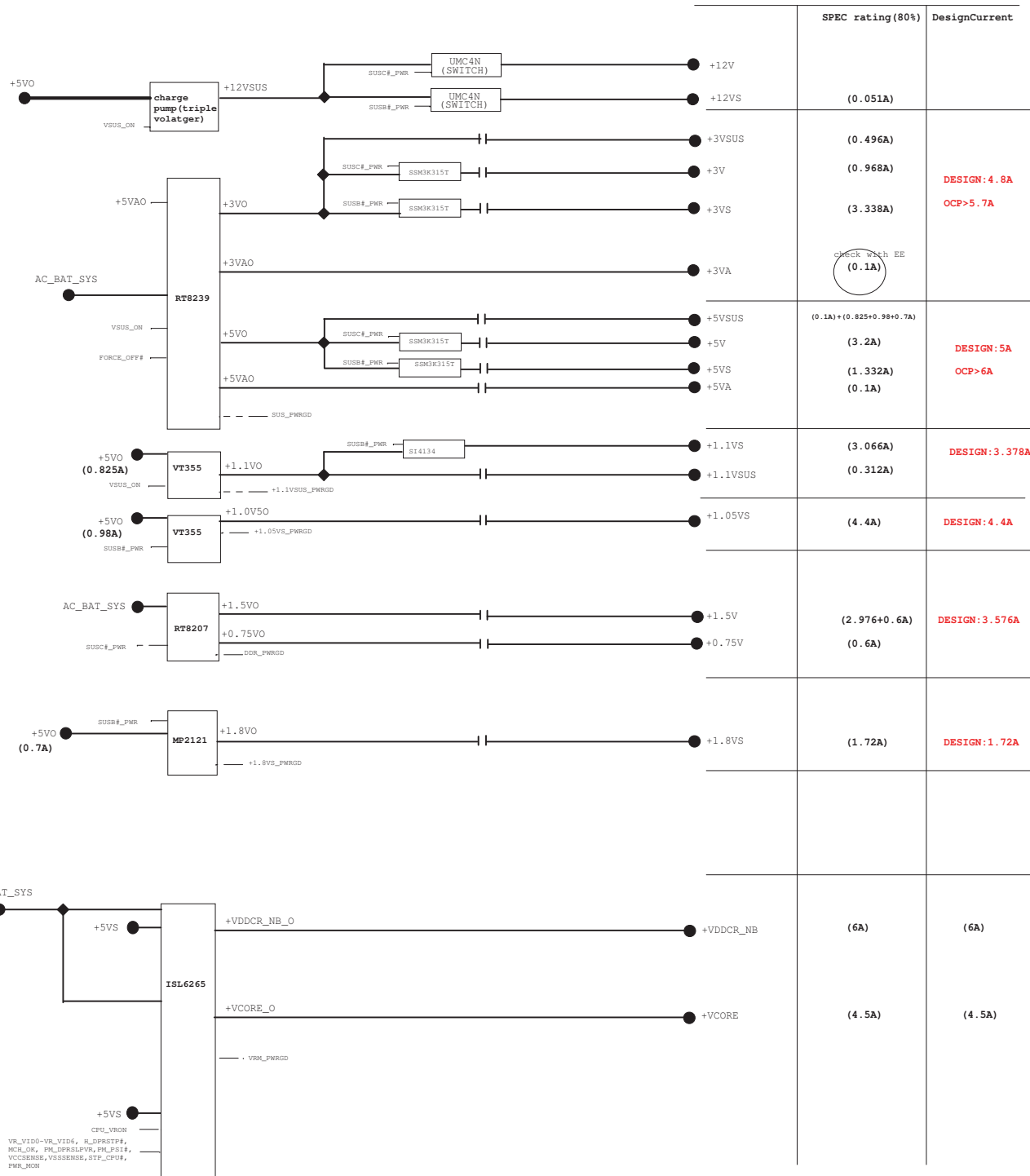


FOR POWER TEST



<Variant Name>

PEGATRON Title :POWER_SIGNAL		
Engineer: <i>Louis</i>		
Size B	Project Name EAB00	Rev 1.0
Date: Tuesday, January 25, 2011	Sheet 93	of 99



SPEC rating (80%)	DesignCurrent
(0.051A)	
(0.496A)	DESIGN: 4.8A OCV>5.7A
(0.968A)	
(3.338A)	
(0.1A) <small>check with EE</small>	
(0.1A)+(0.825+0.98+0.7A)	DESIGN: 5A OCV>6A
(3.2A)	
(1.332A)	
(0.1A)	
(3.066A)	DESIGN: 3.378A
(0.312A)	
(4.4A)	DESIGN: 4.4A
(2.976+0.6A)	DESIGN: 3.576A
(0.6A)	
(1.72A)	DESIGN: 1.72A
(6A)	(6A)
(4.5A)	(4.5A)

follow U21N
System: UL21F
Charger: Ray M17
Red circle is modify by Scott

by Mohoo @9/29

by Scott @9/29

Change Snubber Resistor to 1206 size by Scott @10/01
modify page93 signal info. by Scott @10/01
Add +5VAO signal in Page81 by Scott @10/01

PEGATRON		Title : Power History	
BG1		Engineer: Alfie_Wang	
Size Custom	Project Name EAB00	Rev 1.2	
Date: Tuesday, January 25, 2011		Sheet 95 of 99	

Power On Sequence Diagram

