
COLOR TELEVISION TRAINING MANUAL



FILE NO.

Chassis Series VB8B

CIRCUIT DESCRIPTION

- > **Scan Velocity Modulation Circuit (SVM)**
- > **Right and Left Unbalanced Pincushion Correction Circuit**
- > **Inner Linearity Compensation by Dynamic S-Correction**
- > **Dynamic Focus Circuit**

Note:

The VB8B chassis series is used for flat screen televisions which includes models DS27910 and DS32920 and is similar to the VB7C chassis. This manual contains only the different circuit descriptions from the VB7C chassis. For the complete circuit descriptions refer to the VB7C training manual reference number TI780010.

REFERENCE NO. **TI780011**

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1. Chassis Summary

Fig. 1-1 shows a fundamental block diagram of the VB8B chassis.

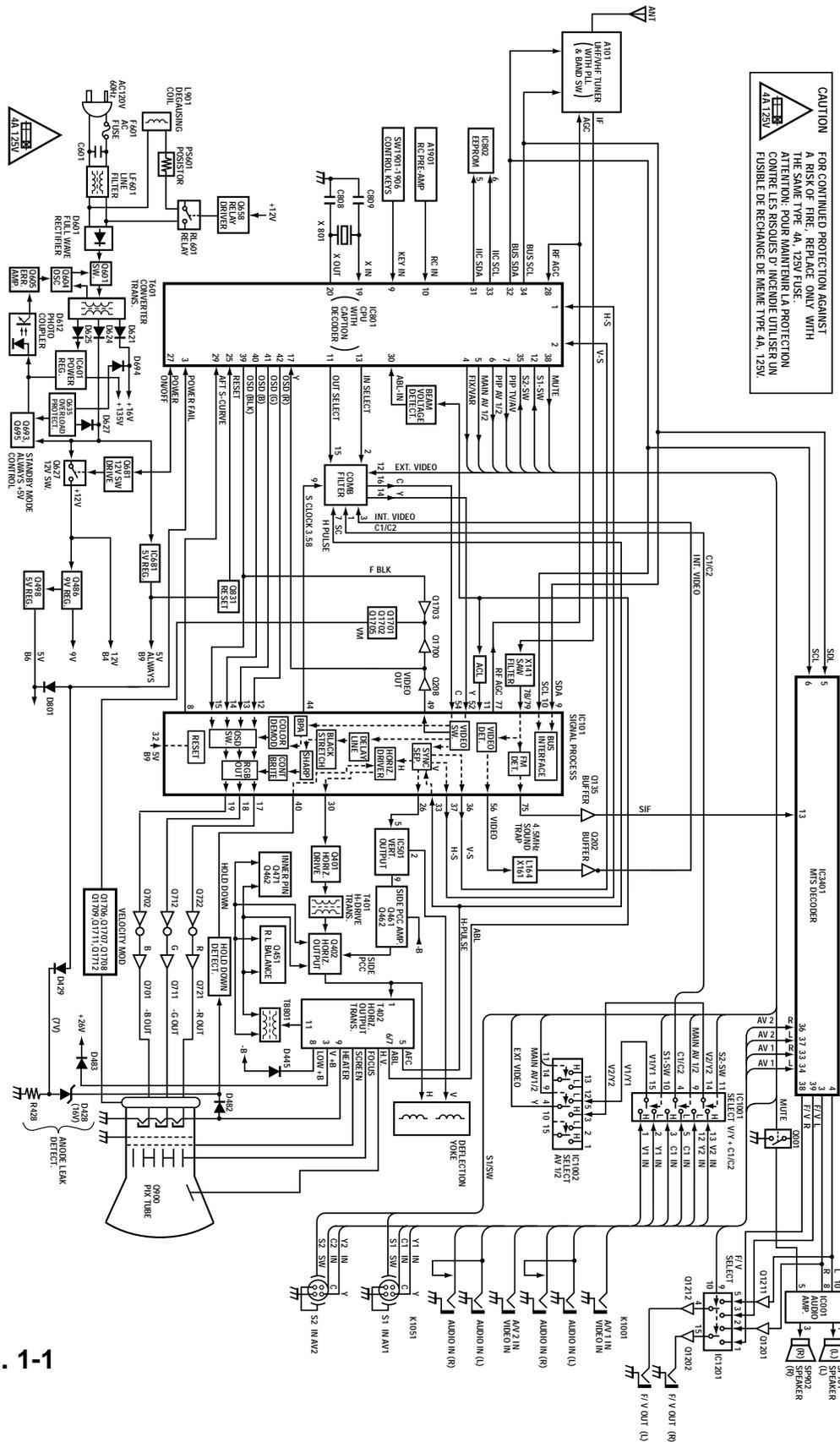


Fig. 1-1

2. Scan Velocity Modulation Circuit (SVM)

2-1 Outline

The SVM (Scan Velocity Modulation) circuit improves the picture resolution by changing the electron beam scan velocity to emphasize the brightness change of the contour of the picture. Increasing the scan velocity of the electron beam makes the activation period of the fluorescent face shorter, lowering brightness. Decreasing scan velocity, increases the period of activation and raises brightness. Because this system does not change the volume of the beam current itself, it does not degrade the focus quality.

Fig. 2-1 shows the SVM circuitry of the VB8B chassis, Fig. 2-2 shows the functional waveforms respectively, and Fig. 2-3 shows the SVM block diagram.

2-2 Operation

At the SVM circuitry, the input video signal with positive polarity (a) is amplified and inverted by Q1701. After passing through Q1702, the signal is differentiated by R1711 and L1701 and becomes (b). This 1st differential signal passes through Q1705 and is further shaped by C1708, C1709, L1702, and R1717, and amplified by Q1706. The result is the current waveform (c) which flows in the SVM coil.

Q1707 and Q1708 compose a complementary-amplification circuit connected directly at the base. The base clipping provided by Q1707 and Q1708 V_{BE} eliminates the fundamental noise generated as a result of primary differentiation and improves the signal-to-noise ratio.

Q1709 and Q1711 compose a class B push-pull current-amplification circuit. The voltage at the connection points of the two output transistor collectors is balanced by half of the 130V source voltage. Direct feedback is applied to the two output transistors by R1736. In operation, when the negative direction modulation voltage is applied to the output circuitry, Q1709 conducts and current flows into the SVM coil charging C1722. At this time the deflection speed is increased and the brilliance decreases.

Next, when the positive direction modulation voltage is applied to the output circuitry, Q1711 conducts and current flows through the SVM coil discharging C1722. At this time, the deflection speed is decreased and the brilliance increases.

The current is 2nd differentiated by the SVM coil and C1722. The SVM coil consists of two coils assembled in the DY/CPM (Convergence Purity Magnet), which is located on the CRT neck and positioned over the electron beam gun. One coil is positioned on the upper side of the gun and the other one is at the lower side of the gun. The current through the SVM coil generates a magnetic field at right angles with the electron beam and is added to the electromagnetic field produced by the horizontal deflection yoke. Thus the deflection velocity of the electron beam is modulated by the SVM magnetic field resulting in a change of brightness. The total horizontal deflection magnetic field applied to the electron beam results in waveform (d). The horizontal electron beam velocity changes as shown in (e) and the resultant brightness change is shown in (f).

When OSD (On Screen Display) characters are displayed, including captions, the blanking pulse is added to transistor Q1701 by Q1703 stopping the SVM so the characters will not be distorted.

Note:

This SVM circuitry is designed to be most effective at a frequency range of 3MHz to 4 MHz of the video signal where the resolution of the picture is most visible.

Fig. 2-1

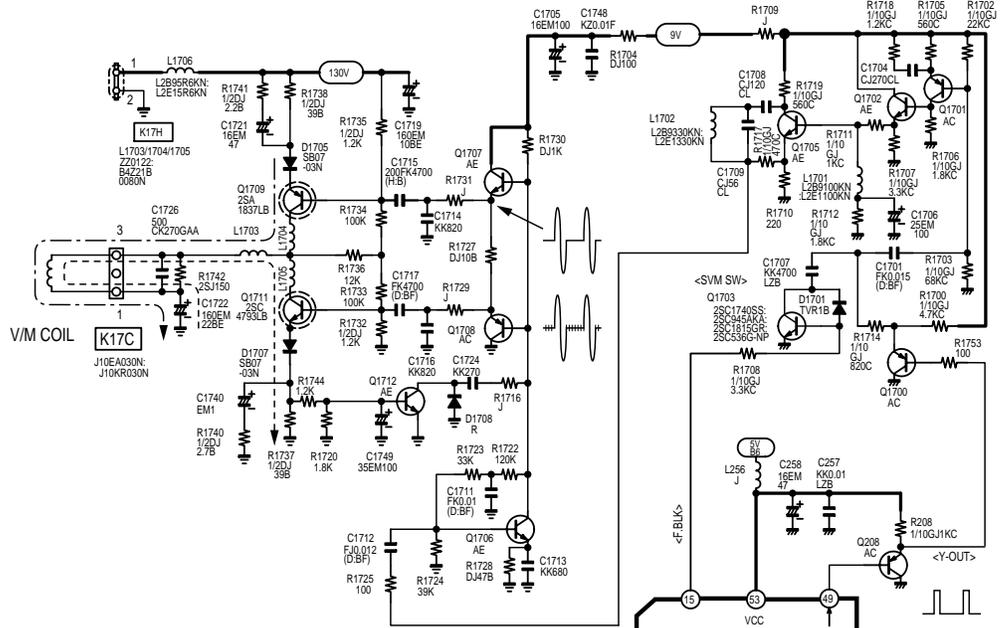


Fig. 2-2

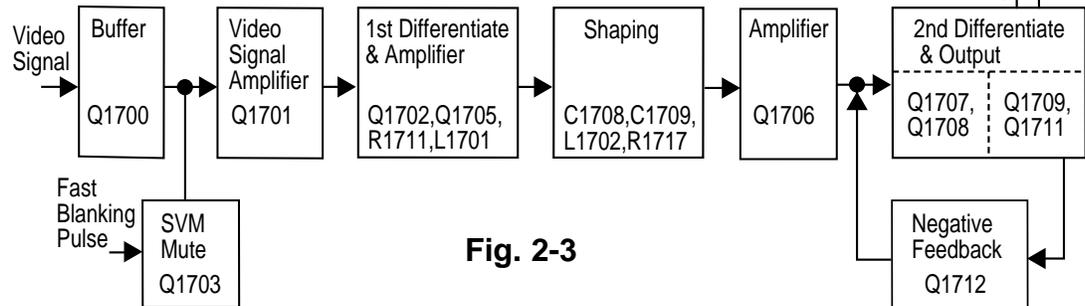
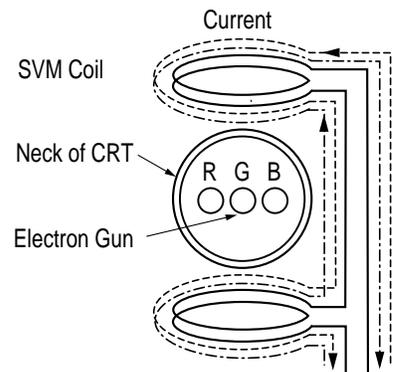
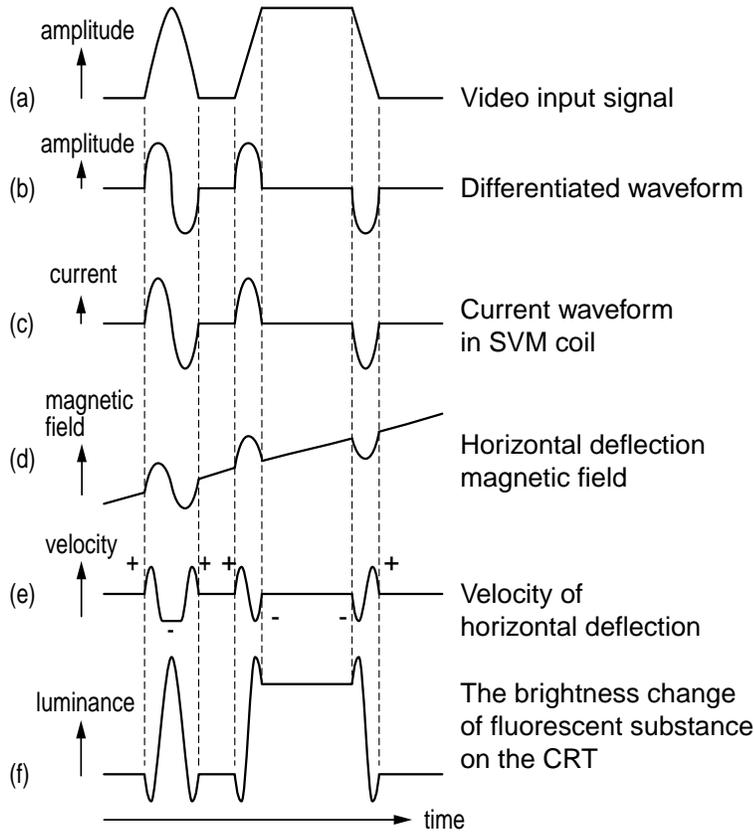
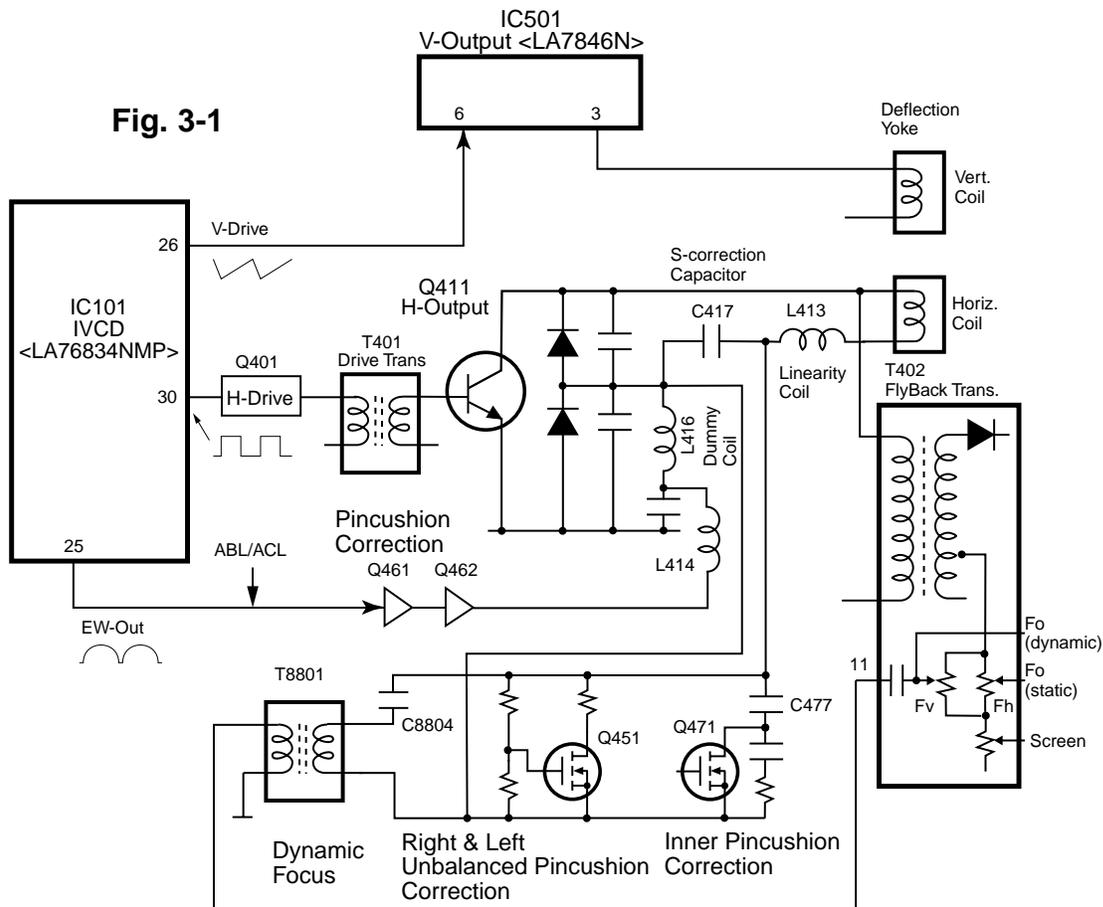


Fig. 2-3

3. Deflection Circuit

3-1 Outline

Fig. 3-1 shows the block diagram of the deflection circuit of VB8B Chassis.



The horizontal drive pulse is output from pin 30 of IC101 (signal processor) and input to the horizontal output stage. The vertical sawtooth signal is output from pin 26 of IC101 and input to pin 6 of IC501. The vertical output signal is output from pin 3 of IC501.

The signal processor (IC101) is controlled and compensated for V-size, S-correction, V-linearity, Pin distortion correction, H-size and H-shift by the CPU via the I²C bus.

Pincushion correction (PCC) is accomplished by adding the east-west parabola pulse output from pin 25 to the horizontal output circuit.

Inner pincushion correction (Inner PCC) and right & left pincushion unbalance correction are accomplished by using FETs in parallel with C417, the S-correction capacitor.

Dynamic focus is also accomplished using T8801 in parallel with the S-correction capacitor C417.

3-2 Pincushion Correction

In the PCC correction circuit, consisting of Q461 and Q462, the east-west parabola signal supplied from pin 25 of IC101 is added at the horizontal output stage and pincushion correction is performed by varying the DC bias.

Further, the ABL and ACL voltage is fed back to the base of Q461 to compensate for the width change by the beam current.

Fig. 3-2 shows a deflection circuit diagram of VB8B chassis

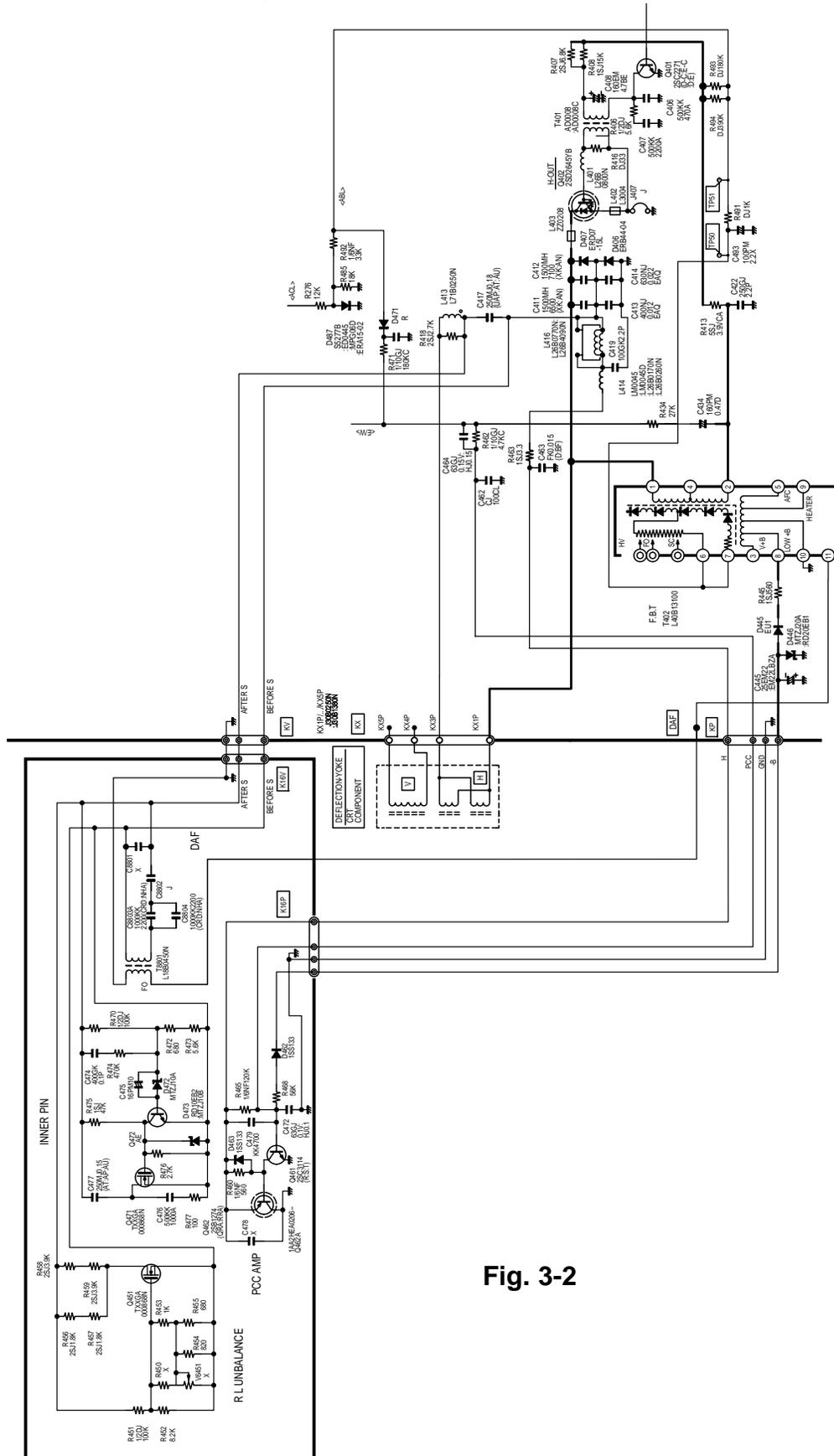


Fig. 3-2

3-3 Right and left unbalanced pincushion correction circuit

3-3-1 Outline

The DY and CPM are adequate for landing the electron beam on the fluorescent screen after passing through the shadow mask. However, as for the pathway of the electron beam, unbalance of right and left occurs because of pincushion distortion. Particularly in the flat face CRT, the unbalanced pincushion distortion can stand out as shown in Fig. 3-6-1.

This is because the migration length of the electron beam is different between the central part and the corner parts of the CRT face.

Generally, conventional pincushion correction circuitry can correct the isometric distortion, but it cannot correct pincushion distortion that is right and left unbalanced.

This unbalanced pincushion correction circuit is constructed with a FET (field effect transistor) and a resistance circuit which are connected in parallel with the S-correction capacitor to resolve the unbalanced pincushion distortion.

3-3-2 Operation

Fig. 3-3 shows the diagram of the right and left unbalanced pincushion correction circuit.

When the S-correction capacitor is charged by the horizontal deflection current i_a in the polarity as shown by the arrow in Fig. 3-3, a positive voltage is impressed between G (gate) and S (source) of the FET by the bias circuit. The FET turns ON between D (drain) and S (source) and current flows according to the voltage across the S-correction capacitor.

When the S-correction capacitor begins to discharge and the bias voltage between gate and source of the FET becomes lower than the threshold level the FET turns OFF.

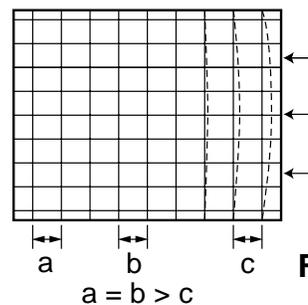
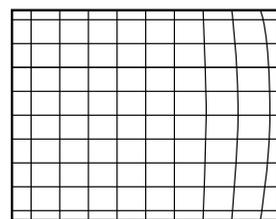
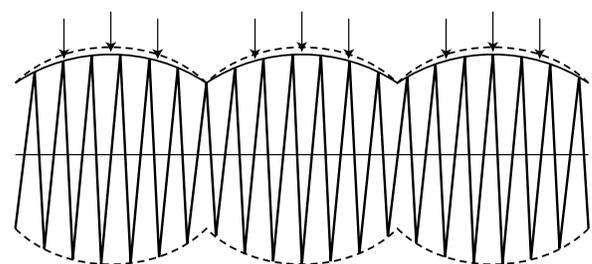
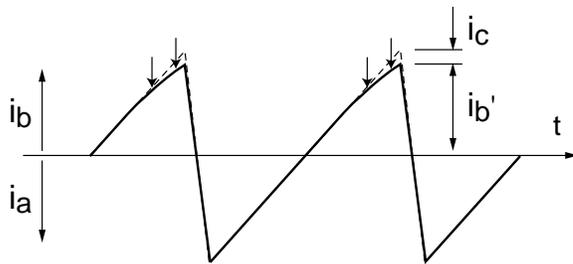
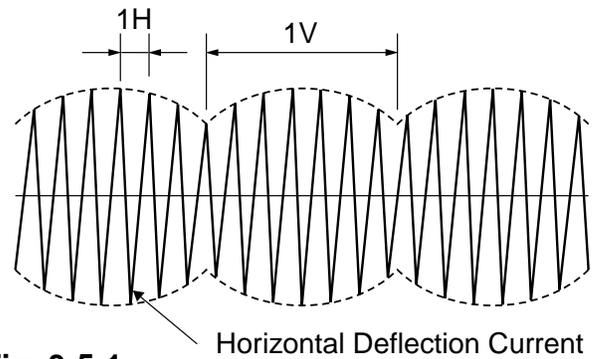
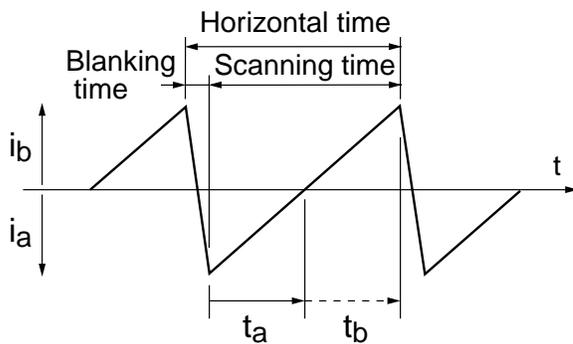
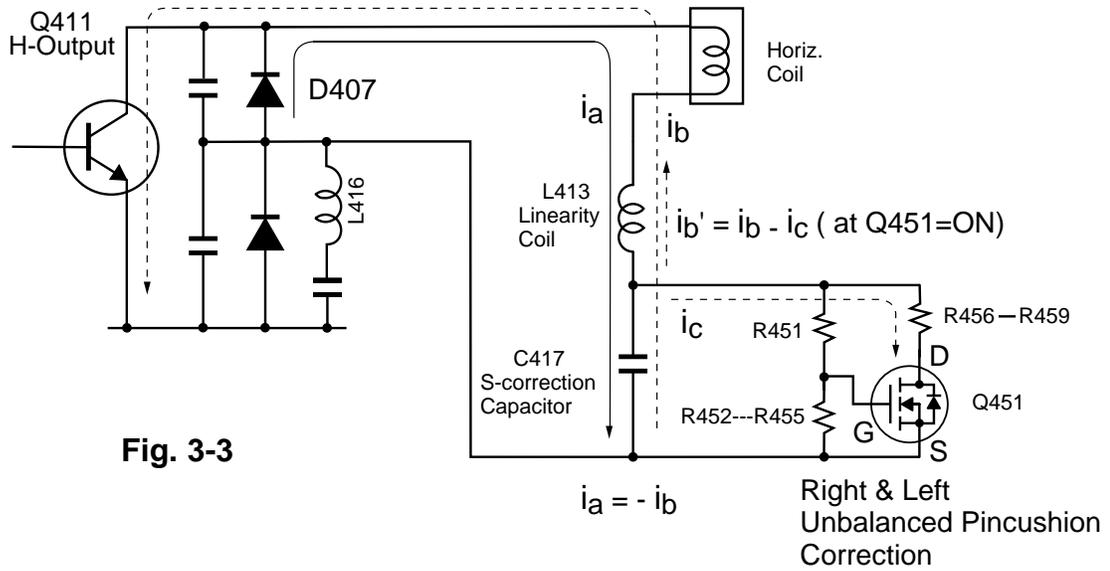
Fig. 3-4-1 and Fig. 3-4-2 show the waveforms of the horizontal deflection current during the horizontal scan period. In the scanning interval last half the horizontal deflection current decreases so that the discharge current from the S-correction capacitor flows towards the FET, and amplitude of the upper part of horizontal deflection current becomes less.

Fig. 3-5-1 and Fig. 3-5-2 show the waveforms of horizontal deflection current in the vertical scan period. When the voltage impressed across the S-correction capacitor is high due to the horizontal deflection current being high, the FET current will become high. This results in the greatest amount of correction. Therefore, the middle of the envelope of the upper part of horizontal deflection current becomes dented as shown in Fig.3-5-2.

Because of this, deflection of the right side of the image becomes less, and the middle of the right side of the image becomes dented as seen in Fig. 3-6-2. In this way the distorted image, which is right and left unbalanced as shown in Fig. 3-6-1, is corrected as shown in Fig. 3-6-2.

Note:

Since correction of the right and left unbalanced pincushion will make the right side of the image smaller than the left side, additional consideration should be given to the linearity coil.



3-4. Inner Linearity Compensation by Dynamic S-Correction

3-4-1 Outline

Generally, a flat picture tube has a geometric error that is called “inner pin distortion.” Inner pin distortion is a geometric error resulting in a different cross hatch width between the sides and the center of the image as shown in Fig. 3-8-1.

Compensating for this error is almost impossible by conventional PCC circuits. This inner pin distortion can be overcome by adapting the value of the S-correction capacitor during a certain interval of the scan time. In this way an improved S-shaped deflection current can be realized to compensate for the above mentioned error of any picture tube.

3-4-2 Operation

Fig. 3-7 shows the diagram of the inner pincushion correction circuit.

Perfect horizontal linearity can be realized by a continuous adaptation of the deflection current during the horizontal scan. Creating a more linear deflection current during the start and end of the scanning time can be realized simply by increasing the value of the S-correction capacity during these scan intervals.

This is accomplished by switching another S-correction capacitor (C477) in parallel with C417 during the proper scan interval or duty cycle.

Generally, the horizontal width is dependent on the voltage across the S-correction capacitor. Therefore, by modulating this voltage the envelope of the horizontal deflection current becomes parabola shaped.

At the vertical scanning time of the top and bottom corners the voltage across the S-correction capacitor is low. At the vertical scanning time of the center part the voltage across the S-correction capacitor is high.

When the voltage across the S-correction capacitor C417 is low, D472 is OFF, Q451 is OFF, Q471 is ON and C477 serves as the additional S-correction capacitor, and the horizontal width is widened.

When the voltage across the S-correction capacitor C417 is high, D472 is ON, Q451 is ON, Q471 is OFF and C477 is removed, and the horizontal width is not changed.

In this way the inner linearity can be fully compensated over the complete picture by modulating the duty cycle as a frame period.

Fig. 3-9-3 shows the horizontal deflection current with the inner Pincushion correction circuit and Fig. 3-8-4 shows the picture after geometrical adjustment.

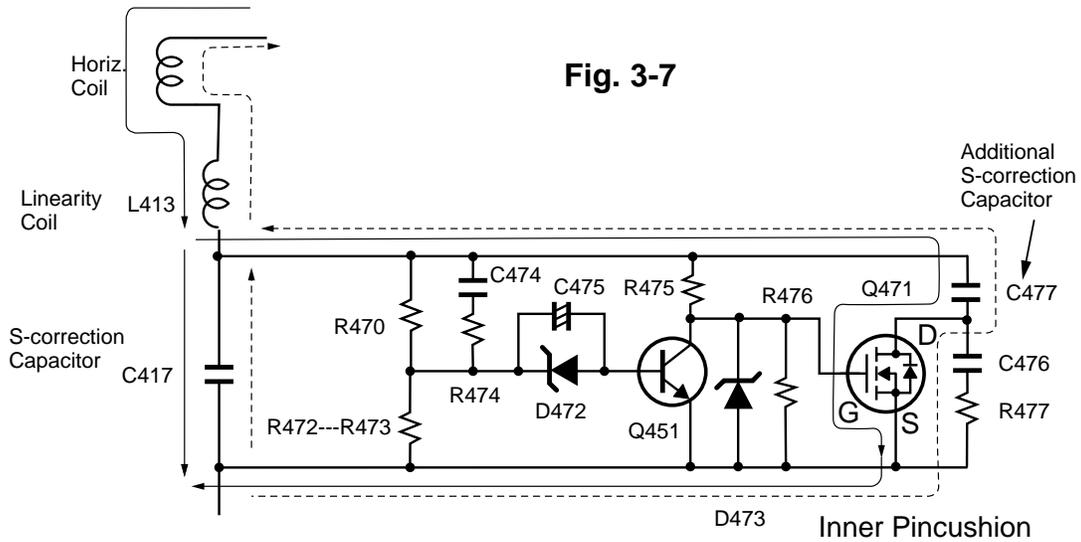
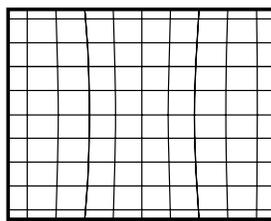
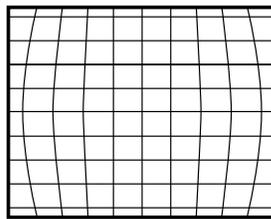


Fig. 3-7



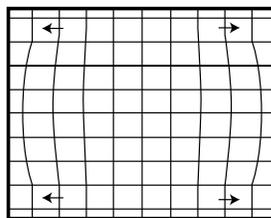
Without Inner Pincushion Correction
(the best adjustment)
corner = straight
center = pin

Fig. 3-8-1



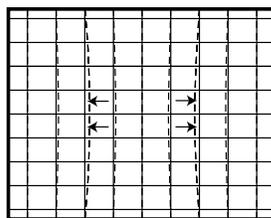
Without Inner Pincushion Correction
corner = barrel
center = straight

Fig. 3-8-2



With Inner Pincushion Correction
The corners are widened.

Fig. 3-8-3



After Geometric Adjustment

Fig. 3-8-4

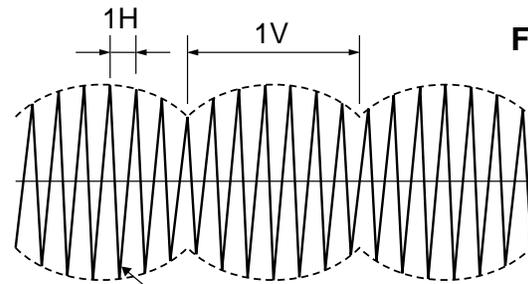


Fig. 3-9-1

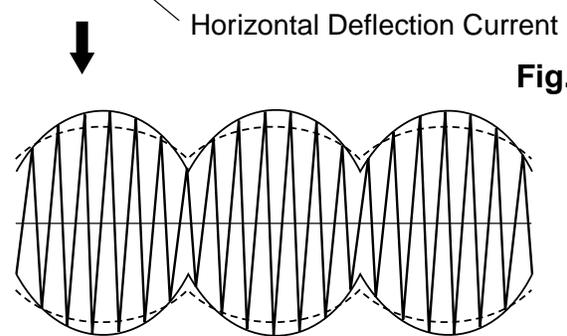


Fig. 3-9-2

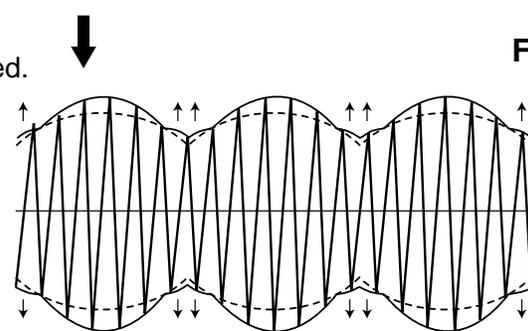


Fig. 3-9-3

4. Dynamic Focus Circuit

4-1 Outline

The migration length of the electron beam is different between the central part and the four corners of the screen. This difference is further increased in a flat face CRT compared to a conventional round shaped CRT. The most suitable focus voltage is usually different according to the migration length of the electron beam. Therefore, it is necessary to change the focus voltage according to the beam landing position to achieve optimum focus. This is called "DAF" (Dynamic Astigmatism Focusing).

The optimum focus voltage waveform is a parabola shape in the horizontal and vertical periods

(Fig. 4-2). Dynamic focus is realized by superimposing the amplified deflection current wave upon the focus electrode.

4-2 Operation

The parabola voltage of the horizontal period is impressed across the S-correction capacitor C417 and coupled by C8803A and C8804 to the primary of T8801. Any DC voltage component is blocked by C8803A and C8804. The parabola voltage is boosted up to approximately 1000V at the secondary coil of the step-up transformer T8801. The parabola voltage is supplied to FBT T402 pin 11 and superimposed upon the DC voltage through the coupling capacitor in the FBT.

The static focus voltage and the dynamic focus voltages are supplied to their respective focus electrodes of the CRT.

Note:

The vertical parabola correction function is not used in the VB8B chassis.

For example, on the specification of CRT A68ERF031X013, the dynamic focus voltage is as follows:

Line parabola (screen edge-to-edge) on $V_{\text{dyn}} = \text{typ. } 800\text{V}$ ---horizontal focus voltage

Frame parabola on $V_{\text{dyn}} = \text{typ. } 350\text{V}$ ---vertical focus voltage

Because the specification for the CRT shows the voltage for effective image screen, it is different from the actual voltage and is more than 1000V as horizontal parabola voltage.

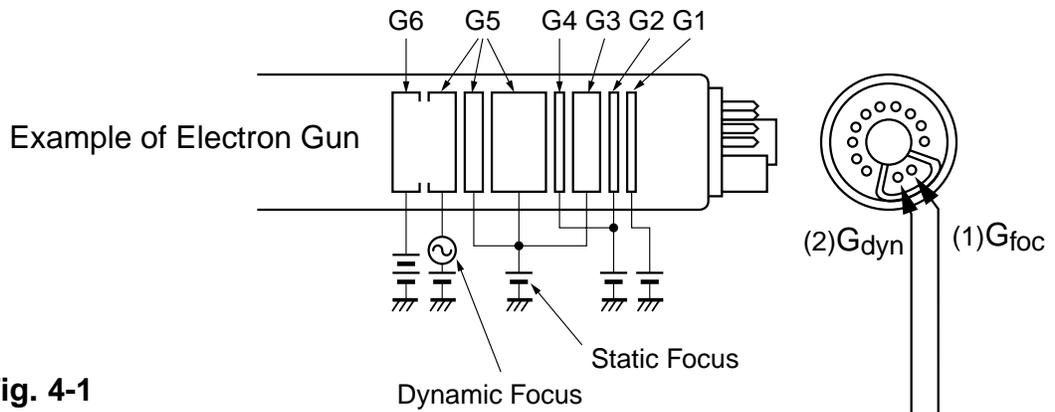


Fig. 4-1

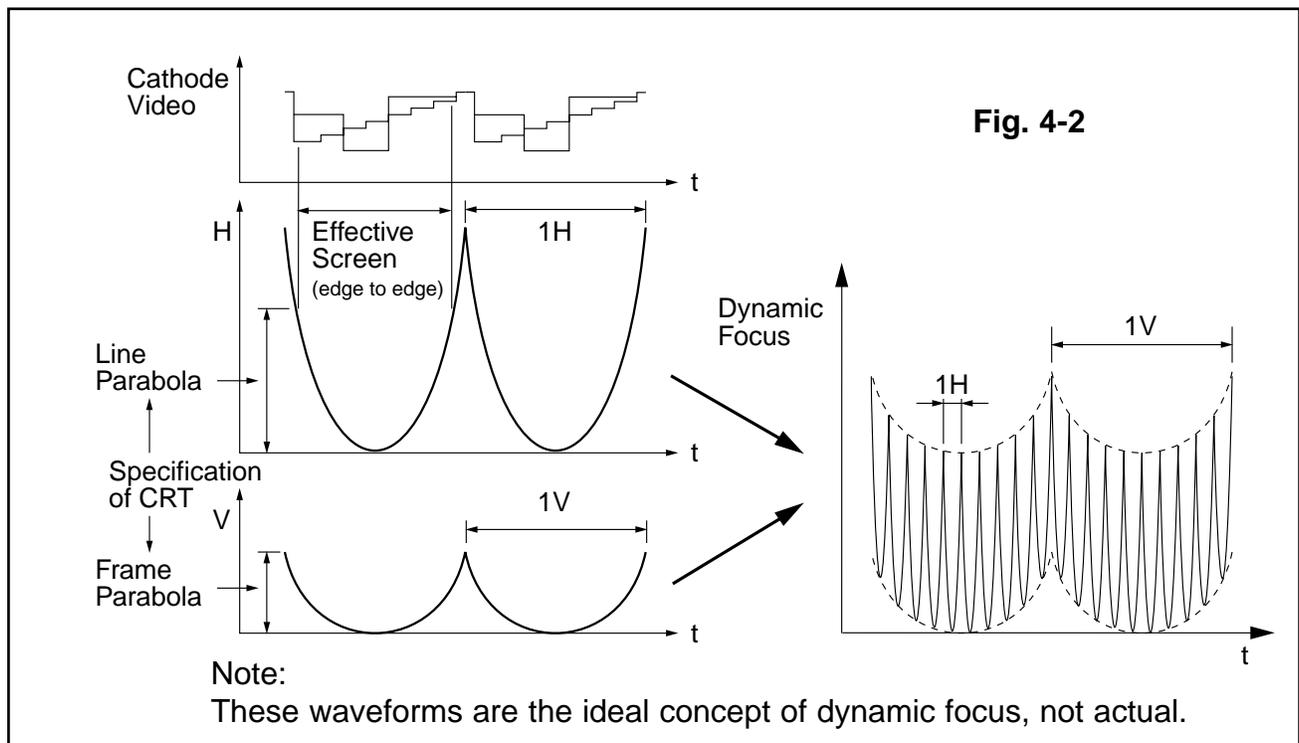
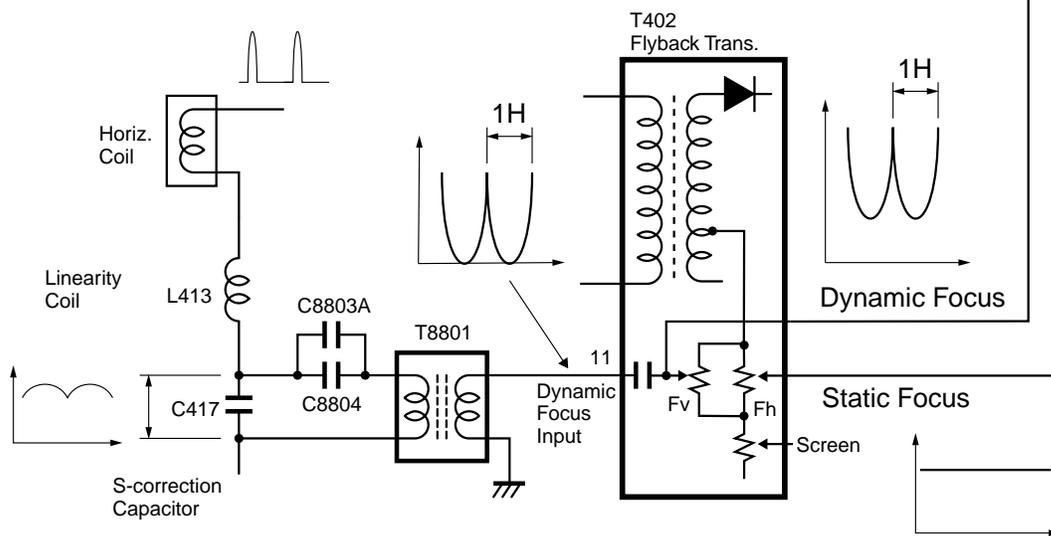


Fig. 4-2

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